LAMPIRAN

```
uses newdelay,crt;
const pa=$300; {inisialisai PPI}
      pb=$301;
      pc=$302;
      pcw=$303;
      cw=$98;

var data,status:byte; {identifikasi variabel}
    s:integer;
    busy:boolean;
    suhu: real;
    tegangan:real;
    tom:char;


begin
clrscr;

TEXTCOLOR(11);
GOTOXY(18,5);writeln('TERMOMETER DIGITAL DENGAN TAMPILAN
KOMPUTER');
gotoxy(18,6);writeln('----------------------------------------');
gotoxy(20,8);write('Set suhu untuk mematikan pemanas=');readln(s);
port[pcw]:=cw; {set control word}
repeat
  port[pc]:=$02;{set PC1 untuk read='1' dan PC0 untuk write='0'
                 pada ADC}
  port[pc]:=$03;  {set PC1 untuk read='1' dan PC0 untuk write='1'
                   pada ADC}

  repeat
  status:=(port[pc] AND $10);{mengecek interupt pada PC4}
  busy:=(status=$01);

  until not (busy);
  port[pc]:=$01;{baca data pad port A}
  data:=port[pa];
  suhu:= ( data*0.69736421) +26;{konversi data ke suhu}
```

```
delay(2);

Port[pc]:=$03;{start konversi lagi}
textcolor(11);

textcolor(7);gotoxy(30,10);writeln('DATA:',DATA:3);
GOTOXY(30,13);writeln('TEMPERATUR:',suhu:3:0);


textcolor(11);
gotoxy(19,17);writeln('-------------------------------------');

if s<=suhu then {jika input lebih kecil dari suhu maka port B
begin           high}
port[pb]:=$1;
textcolor(4+blink);
gotoxy(20,20);writeln('pemanas mati');
end
else  {jika tidak maka pemanas hidup}
port[pb]:=$0;
if keypressed then tom:=readkey;
until tom=#27;
end.
```

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5 \times 10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\ (\text{Volts/Sec}) = \frac{I_L(pA)}{C_H(pF)}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100pA}{100pF} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt:

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{t_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dt}$ in the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

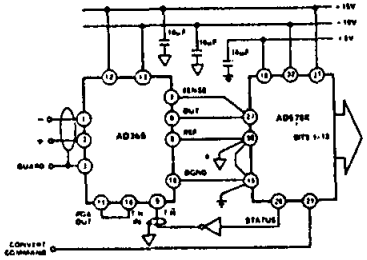


Figure 23. A D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

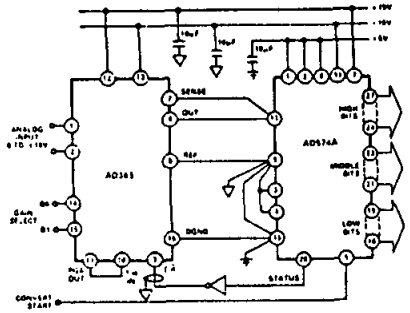


Figure 24. 12-Bit A D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

ANALOG DEVICES

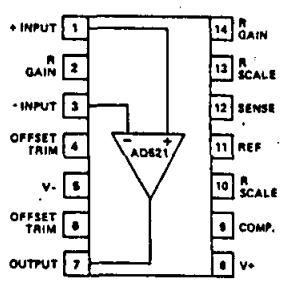
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

- Programmable Gains from 0.1 to 1000
- Differential Inputs
- High CMRR: 110dB min
- Low Drift: 2μV/°C max (L)
- Complete Input Protection, Power ON and Power OFF
- Functionally Complete with the Addition of Two Resistors
- Internally Compensated
- Gain Bandwidth Product: 40MHz
- Output Current Limited: 25mA
- Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
- Chips are Available

AD521 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance (3 X $10^9\,\Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD2115D/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	•	•	•
Equation	$G = R_S/R_G$ V/V	•	•	•
Error from Equation	(±0.25 +0.004G)%	•	•	•
Nonlinearity (Note 2)				
1≤G≤100	0.2% max	•	0.1% max	•
Gain Temperature Coefficient	±(5 ±0.05G)ppm/°C	•	•	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	•	•	•
Output at Maximum Operating Temperature	±10V @ 5mA min	•	•	•
Impedance	0.1Ω	•	•	•
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	> 2MHz	•	•	•
G = 10	300kHz	•	•	•
G = 100	200kHz	•	•	•
G = 1000	40kHz	•	•	•
Small Signal, ±1.0% Flatness				
G = 1	75kHz	•	•	•
G = 10	26kHz	•	•	•
G = 100	24kHz	•	•	•
G = 1000	4kHz	•	•	•
Full Peak Response (Note 3)	100kHz	•	•	•
Slew Rate, 1≤G≤1000	10V/µs	•	•	•
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7µs	•	•	•
G = 10	5µs	•	•	•
G = 100	10µs	•	•	•
G = 1000	35µs	•	•	•
Differential Overload Recovery (±30V input to within 10mV of Final Value) (Note 4)				
G = 1000	50µs	•	•	•
Common Mode Step Recovery (30V input to within 10mV of Final Value) (Note 5)				
G = 1000	10µs	•	•	•
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	••
vs. Temperature	15µV/°C max (7µV/°C typ)	5µV/°C max (1.5µV/°C typ)	2µV/°C max	••
vs. Supply	3µV/%	•	•	•
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	••
vs. Temperature	400µV/°C max (150µV/°C typ)	150µV/°C max (50µV/°C typ)	75µV/°C max	••
vs. Supply (Note 6)	$0.005\% V_{OS_O}/\%$	•	•	•
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	••	••
vs. Temperature	1nA/°C max	500pA/°C max	••	••
vs. Supply	2%/V	•	•	•
Input Offset Current	20nA max	10nA max	••	••
vs. Temperature	250pA/°C max	125pA/°C max	••	••
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9\Omega$‖1.4pF	•	•	•
Common Mode Input Impedance (Note 8)	$6 \times 10^{10}\Omega$‖1.0pF	•	•	•
Input Voltage Range for Specified Performance (with respect to ground)	±10V	•	•	•
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	•	•	•
Voltage at either input (Note 9)	V_S ±15V	•	•	•
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	••	••
G = 10	90dB min (96dB typ)	94dB min (100dB typ)	••	••
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	••	••
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	••	••
NOISE				
Voltage RTO (p-p) 0.1Hz to 10Hz (Note 10)	$\sqrt{(10\ 5G)^2 + (22)^2}$µV	•	•	•
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}$µV	•	•	•
Input Current, rms, 10Hz to 10kHz	15pA (rms)	•	•	•
REFERENCE TERMINAL				
Bias Current	3µA	•	•	•
Input Resistance	10MΩ	•	•	•
Voltage Range	±10V	•	•	•
Gain to Output	1	•	•	•
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	•	•	•
Quiescent Supply Current	5mA max	•	•	•
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	•	•	-55°C to +125°C
Operating	-25°C to +85°C	•	•	-55°C to +125°C
Storage	-65°C to +150°C	•	•	•
PACKAGE OPTION[1]				
Ceramic (D-14)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES
[1] See Section 16 for package outline information.
*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

Applying the AD521

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10µs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10µs pulse at a 1kHz rate. (When a common mode signal greater than V_S -0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 seperate 10 second periods with the test circuit of Figure 8.

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

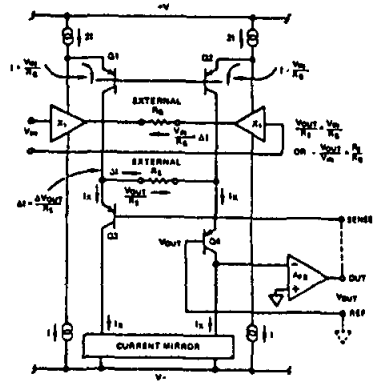


Figure 1. Simplified AD521 Schematic

Use the LM158/LM258/LM358 Dual, Single Supply Op Amp

National Semiconductor
Application Note 116
Jim Sherwin

INTRODUCTION

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the LM1458/LM1558 with split supply and reap the profits in terms of:

a. Input and output voltage range down to the negative (ground) rail

b. Single supply operation

c. Lower standby power dissipation

d. Higher output voltage swing

e. Lower input offset current

f. Generally similar performance otherwise

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. Table I shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

SINGLE SUPPLY OPERATION

The LM1458/LM1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

TABLE I. Comparison of Dual Op Amps LM1458 and LM358

Characteristic	LM1458	LM358
V_{IO}	6 mV Max	7 mV Max
CM V_I	24 Vp-p*	0–28.5V*
I_{IO}	200 nA	50 nA
I_{OB}	500 nA	−500 nA
CMRR	60 dB Min @ 100 Hz 90 dB Typ	85 dB Typ @ DC
$\bar{e}_n$ @ 1 kHz, R_{GEN} 10 kΩ	45 nV/$\sqrt{Hz}$ Typ	40 nV/$\sqrt{Hz}$ Typ**
Z_{IN}	200 MΩ Typ	Typ 100 MΩ
A_{VOL}	20k Min 100k Typ	100k Typ
f_c	1.1 MHz Typ	1 MHz Typ**
P_{BW}	14 kHz Typ	11 kHz Typ**
dV_o/dt	0.8V/μs Typ	0.5V/μs Typ**
V_o @ R_L = 10k/2k	24/20 Vp-p*	28.5 Vp-p
I_{SC}	20 mA Typ	Source 20 mA Min (40 Typ) Sink 10 mA Min (20 Typ)
PSRR @ DC	37 dB Min 90 dB Typ	100 dB Typ
I_D (R_L = ∞)	8 mA Max	2 mA Max

‡From laboratory measurement

*Based on V_S = 30V on LM358 only, or V_S = ±15V

**From data sheet typical curves

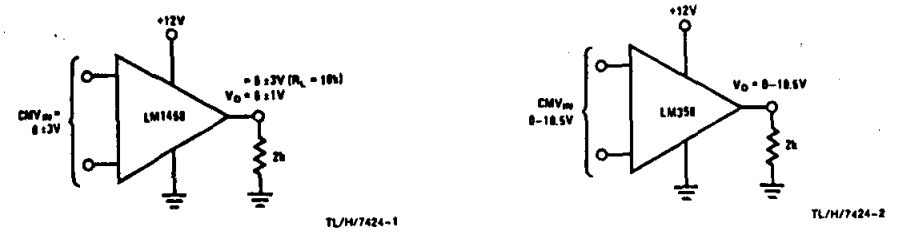


FIGURE 1. Worst Case Signal Levels with + 12V Supply

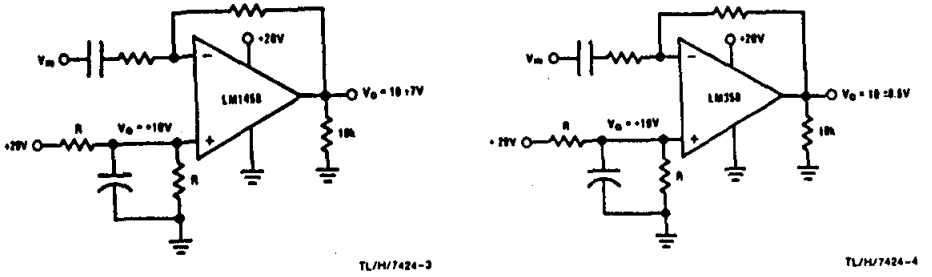


FIGURE 2. Operating with AC Signals

AC GAIN

For AC signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the LM1458 the quiescent output must be higher, $V_Q \geq 3V + V_{IN}$ pk thus, for small signals, power dissipation is much greater with the LM1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, V_{SUPPLY} = as required. Find quiescent dissipation in load and amplifier for LM1458 and LM358.

LM358	LM1458
$V_Q = +1V$	$V_Q = 4V$
$V_{SUPPLY} = +3.5V$	$V_{SUPPLY} = 8V$
$P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5$ mW	$P_{LOAD} = \frac{4^2}{2k} = 8$ mW
$P_D = V_S I_S' + (V_S - V_O) I_L$	$P_D = P_{D}' + (V_S - V_O) I_L$
$= 3.5V \times 0.7$ mA $+ (3.5-1)\frac{1V}{2k}$	$= 22$ mW $+ (8-4)\frac{4V}{2k}$
$P_D = 2.45 + 1.25 = 3.7$ mW	$P_D = 22 + 8 = 30$ mW
$P_{TOTAL} = 3.7 + 0.5 = 4.2$ mW	$P_{TOTAL} = 30 + 8 = 38$ mW
*From typical characteristics	*From typical characteristics

The LM1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

INVERTING DC GAIN

Connections and biasing for DC inverting gain are essentially the same as for the AC coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

NON-INVERTING DC GAIN

The non-inverting gain connection does not require the V_Q biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore DC signals in the low-millivolt range can be handled. The LM1458 still requires that V_{IN} = 3–17V. Therefore maximum gain is limited to $A_V = (V_O - 3)/3$, or A_V max = 5.4 for a 20V supply.

There is no similar limitation for the LM358.

ZERO T.C. INPUT BIAS CURRENT

An interesting and unusual characteristic is that I_{IN} has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

BALANCED SUPPLY OPERATION

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.

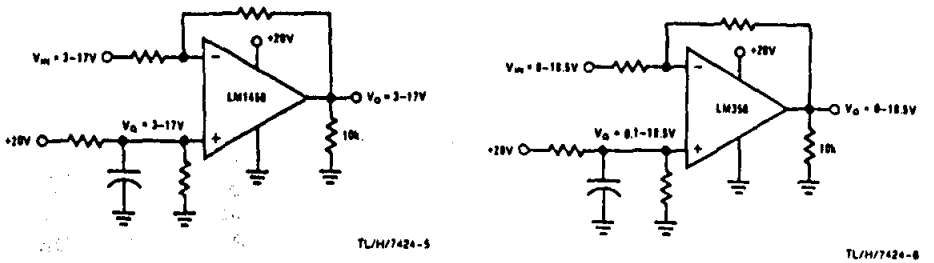


FIGURE 3. Typical DC Coupled Inverting Gain

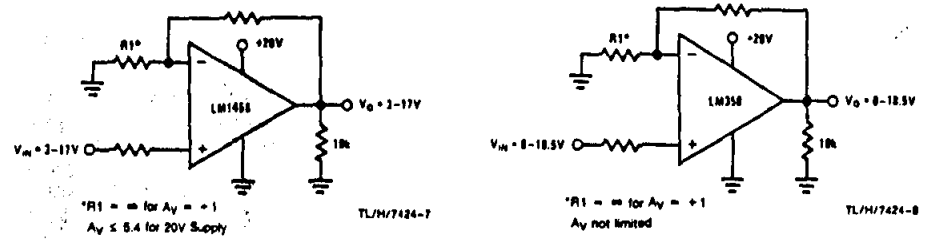


FIGURE 4. Typical DC Coupled Non-Inverting Gain

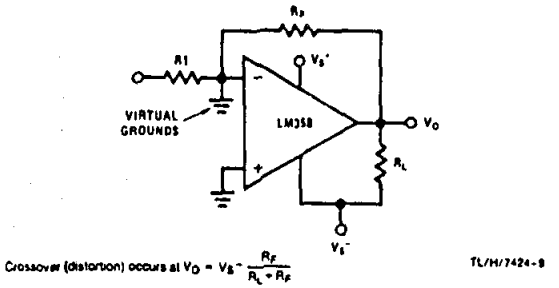


FIGURE 5. Split Supply Operation of LM358

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. R_L to the negative rail should be chosen small enough that the voltage divider formed by R_F and R_L will permit V_O to swing negative to the desired point according to the equation:

$$R_L = R_F \frac{V_S - V_O}{V_O}.$$

R_L could also be returned to the positive supply with the advantage that V_O max would never exceed ($V_S^+ - 1.5V$). Then with ±15V supplies $R_{L\ MIN}$ would be 0.12 R_F. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore R_L to negative supply can be one-half the value of R_L to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, Table II shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference V_O at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

TABLE II. Conventional Op Amp Circuits Suitable for Single Supply Operation

Application	Limitations
AC Coupled amp‡	V_O*
Inverting amp	V_O
Non-inverting amp	OK*
Unity gain buffer	OK
Summing amp	V_O
Difference amp	V_O
Differentiator	V_O
Integrator	V_O
LP Filter	V_O
I-V Connector	V_O
PE Cell Amp	OK
I Source	$I_{O\ MIN} = \frac{1.5}{R1}$
I sink	OK
Volt Ref	OK
FW Rectifier	V_O or modified circuit
Sine wave osc	V_O
Triangle generator	V_O
Threshold detector	OK
Tracking, regulator PS	Not practical
Programmable PS	OK
Peak Detector	OK to $V_{IN} = 0$

‡See AN20 for conventional circuits

*V_O denotes need for a reference voltage, usually at about $\frac{V_S}{2}$

OK means no reference voltage required

LF 355N, LF 356N, LF 357N
Penguat Operasi Masukan JFET
(JFET Input Operational Amplifiers)

Penguat-penguat operasi ini memiliki transistor-transistor masukan JFET, dengan arus-arus gelincir dan arus-arus masukan sangat kecil. Keluarannya dirancang untuk beban bersifat kapasitas tinggi tanpa sesuatu persoalan stabilitas.

Sifat-sifat tambahan:

- Resistansi masukan sangat tinggi
- Sedikit hanyut oleh perubahan suhu
- Lebarjalur lebar
- Dibolehkan tegangan masukan tinggi sampai $+V_s$
- Konpensasi frekuensi intern

Tarif Maksimum

Tegangan catu	V_S	±18		V
Tegangan *masukan diferensial*	V_{iD}	±30		V
Lama hubungsingkat keluaran	t_{osc}	∞		
Jangkah suhu simpan	T_s	−55	−125	°C
Suhu pertemuan	T_j	100		°C
Resistansi termik antara sistem-udara lingkungan	$R_{th\,j\text{-}amb}$	175		K/W

Konfigurasi pena

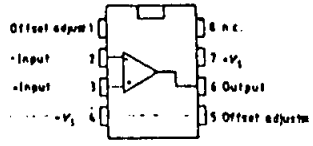
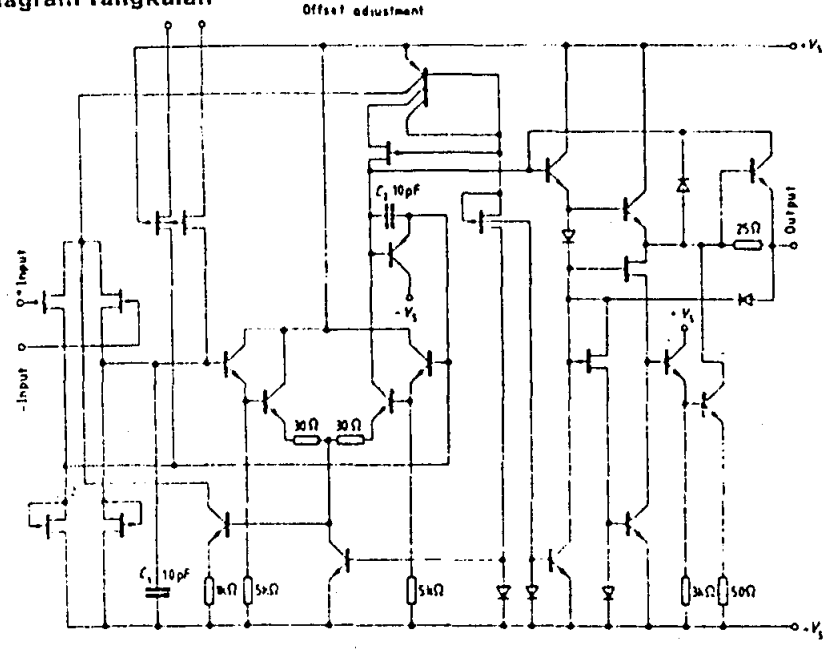


Diagram rangkaian



Karakteristik

V_S = ±15 V, T_{amb} = 25 °C			min	typ	max	
Open loop supply current consumption	LF 355 N	I_S		2	4	mA
	LF 356 N, LF 357 N	I_S		5	10	mA
Input offset voltage	(R_G = 50 Ω)	V_{IO}		3	10	mV
Input offset current		I_{IO}		3	50	pA
Input current		I_I		30	200	pA
Input resistance		R_I		10^{12}		Ω
Open loop voltage gain		A_{VO}		80	106	dB
Rate of rise						
	LF 355 N: A_V = 1	$\frac{dvq}{dtr}$		5		V/µs
	LF 356 N: A_V = 1			12		V/µs
	LF 357 N: A_V = 5			50		V/µs
Performance bandwidth	LF 355 N	f_p		2.5		MHz
	LF 356 N	f_p		5		MHz
	LF 357 N	f_p		20		MHz
Transient time (for 0.01%)						
	LF 355 N	t_r		4		µs
	LF 356 N, LF 357 N	t_r		1.5		µs
Input noise voltage						
R_S=100Ω;f=100 Hz:	LF 355 N	V_{IN}		25		nV/√Hz
	LF 356 N, LF 357 N	V_{IN}		15		nV/√Hz
R_S=100Ω,f=1000 Hz:	LF 355 N	V_{IN}		20		nV/√Hz
	LF 356 N, LF 357 N	V_{IN}		12		nV/√Hz
Input noise current						
f = 100 Hz, or 1000 Hz		I_{IN}		0.01		pA/√Hz
Input capacitance		C_I		3		pF

Karakteristik

V_S = ±15 V; T_{amb} = 0 to 70 °C, unless otherwise specified					
Input offset voltage R_G = 50 Ω	V_{IO}			14	mV
Temperature coefficient of V_{IO}: R_S = 50 Ω	α_{VIO}		5		µV/K
Change of α_{VIO} after a change of V_{IO} adjustment[1]	$\Delta\alpha_{VIO}$		0.5		per mV
Input offset current T_j = 70 °C	I_{IO}			2	nA
Input current[2] T_j = 70 °C	I_I			8	nA
Open loop voltage gain					
R_L = 2 kΩ, V_{Opp} = ±10 V	A_{VO}	63			dB
Output voltage R_L = 10 kΩ	V_{Opp}	12	±13	−12	V
R_L = 2 kΩ	V_{Opp}	10	±12	−10	V
Input common mode range	V_{IC}	+11	+12	−11	V
Common mode rejection	k_{CMR}	80	100		dB
Supply voltage rejection	k_{SVR}	80	100		dB

Catatan:

1) Kalau dibandingkan dengan harga asli yang tak dapat ditepatkan, koefisien suhu dari tegangan gelincir masukan yang telah ditepatkan hanya berubah sedikit (lumrahnya 0,5 µV/K) untuk setiap mV dalam jangkah setan. Penepatan tegangan gelincir tidaklah berpengaruh kepada tindasan ragam tunggal *(common mode rejection)* dan kepada penguatan ikal terbuka.
2) Arus masukan berlipat hampir dua-kali, kalau suhu pertemuan naik 10 K.

pewaktu 555*

appendiks 4

*Ijin dari Signetics Corporation, 811 East Arques, Sunnyvale, California, 94086, hakcipta 1974.

URAIAN

Rangkaian Pewaktu monolitik NE/SE 555 adalah pengendali sangat stabil yang berkemampuan menghasilkan penundaan waktu yang teliti, atau osilasi. Bila diperlukan diberikan terminal-terminal tambahan untuk memicu atau mereset. Dalam mode operasi penundaan waktu, waktunya dikendalikan secara tepat oleh satu tahanan luar dan kapasitor. Untuk operasi stabil sebagai sebuah osilator, baik frekuensi bergerak bebas dan siklus tugasnya dikendalikan secara teliti dengan dua tahanan luar dan satu kapasitor. Rangkaiannya bisa dipicu dan direset pada bentuk gelombang yang menurun, dan struktur keluarannya dapat mengeluarkan atau menerima sampai 300mA atau menggerakkan rangkaian-rangkaian TTL.

KEISTIMEWAAN

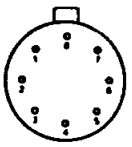
- **TIMING WAKTU DARI MIKRODETIK SAMPAI BEBERAPA JAM.**
- **BEKERJA BAIK PADA MODE STABIL MAUPUN ASTABIL.**
- **SIKLUS TUGAS DAPAT DISETEL**
- **KELUARAN ARUS TINGGI DAPAT MENGELUARKAN ATAU MENERIMA 200mA**
- **KELUARANNYA DAPAT MENGGERAKKAN TTL**
- **KESTABILAN SUHU SEBESAR 0.005% PER °C**
- **KELUARANNYA HIDUP DAN MATI SECARA BIASA**

PEMAKAIAN

PENENTUAN-WAKTU PRESISI
PEMBANGKITAN DENYUT
PENENTUAN WAKTU BERURUTAN
PEMBANGKITAN WAKTU PENUNDAAN
MODULASI LEBAR DENYUT
MODULASI KEDUDUKAN DENYUT
DETEKTOR DENYUT HILANG

KONFIGURASI PASAK (Tampak Atas)

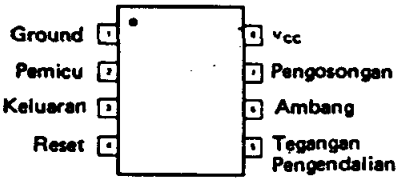
PAKET T



1. Ground
2. Pemicu
3. Keluaran
4. Reset
5. Tegangan Pengendalian
6. Ambang
7. Pembuangan
8. VCC

Nomor-nomor Pesanan SE555T/NE555/

PAKET V

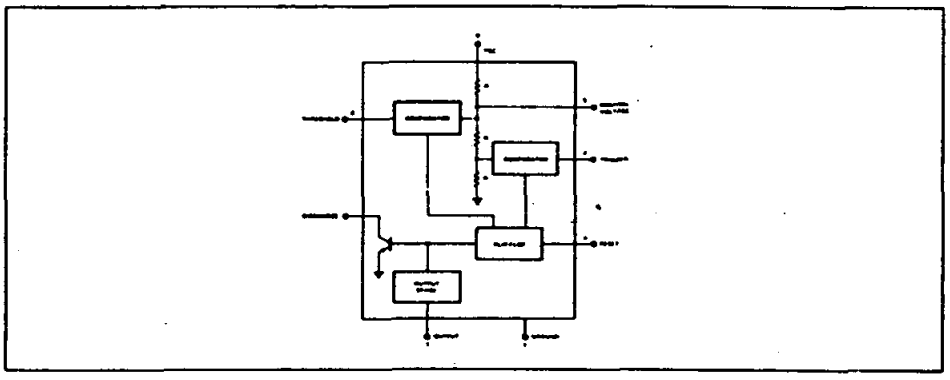


Nomor-nomor Pesanan SE555V/NE555V

RATING MAKSIMUM MUTLAK

Tegangan Suplai	+18V
Penyerapan Daya	600 mW
Jangkauan Suhu Operasi	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Jangkauan Suhu Penyimpanan	−65°C to +150°C
Suhu Timbal (Penyolderan, 60 detik)	+300°C

DIAGRAM BLOK

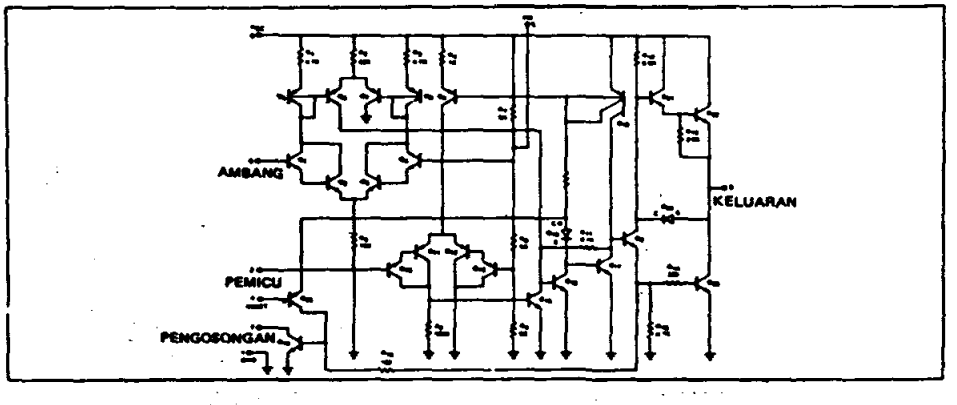


CIRI-CIRI LISTRIK T_A 25°C, V_{CC} = +5 sampai +15 kecuali ditentukan lain

PARAMETER	KONDISI UJI	SE 555			NE 555			SATUAN
		MIN	JENIS	MAKS	MIN	JENIS	MAKS	
Tegangan Suplai		4.5		18	4.5		16	V
Arus Suplai	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Keadaan, rendah, Catatan 1							
Selang Penentuan Waktu (Monostabil)	R_A, R_B = 1KΩ sampai 100kΩ							
Ketelitian Awal	C = 0.1 μF Note 2		0.5	2		1		%
Drift bersama Suhu			30	100		50		ppm/°C
Drift bersama Tegangan Suplai			0.05	0.2		0.1		%/Volt
Tegangan Ambang			2/3			2/3		x V_{CC}
Tegangan Pemicu	V_{CC} = 15V	4.8	5	5.2		5		V
Selang Penentuan Waktu (Astabil)	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Arus Pemicu			0.5			0.5		μA
Tegangan Reset		0.4	0.7	1.0	0.4	0.7	1.0	V
Arus Reset			0.1			0.1		mA
Arus Ambang	Note 3		0.1	.25		0.1	.25	μA
Taraf Tegangan Pengendalian	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Tegangan Keluaran (rendah)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Penurunan Tegangan Keluaran (rendah)								
	I_{SOURCE} = 200mA		12.5			12.5		
	V_{CC} = 15V							
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Waktu Naik untuk Keluaran			100			100		ndetik
Waktu Turun Keluaran			100			100		ndetik

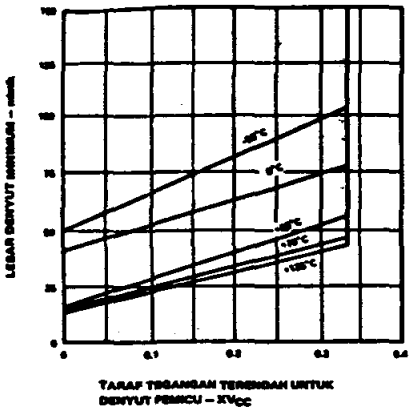
CATATAN
1. Arus Suplai bila keluarannya tinggi biasanya 1mA atau kurang.
2. Diuji di V_{CC} = 5V dan V_{CC} = 15V.
3. Ini akan menentukan harga maksimum dari R_A + R_B. Untuk Operasi 15V, R total maksimumnya = 20 MegaOhm.

RANGKAIAN EKUIVALEN (Diperlihatkan Hanya Satu Sisi Saja)

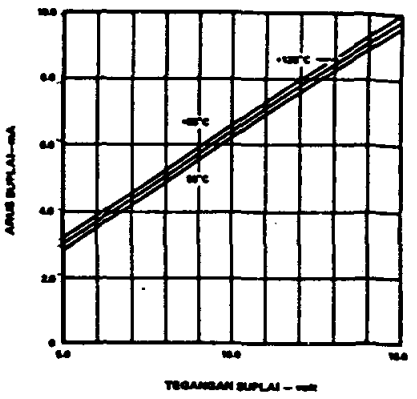


CIRI-CIRI KHAS

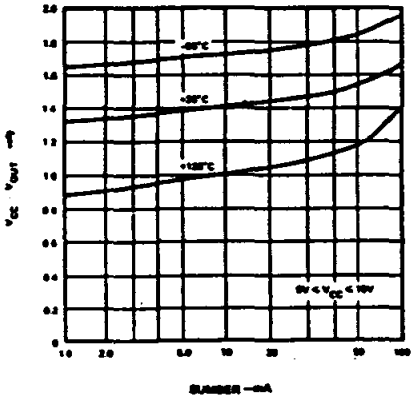
LEBAR DENYUT MINIMUM
YANG DIPERLUKAN UNTUK PEMICUAN



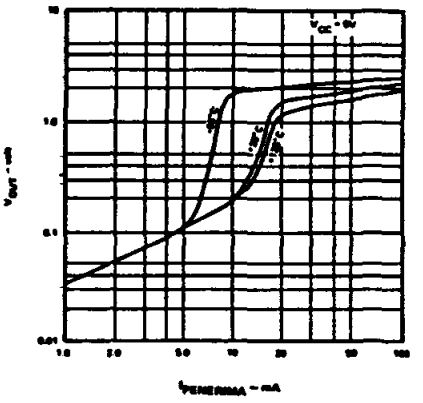
ARUS SUPLAI
vs. TEGANGAN SUPLAI



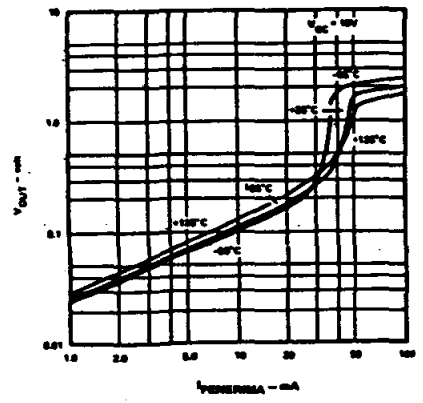
TEGANGAN KELUARAN RENDAH
vs. ARUS PENERIMA KELUARAN



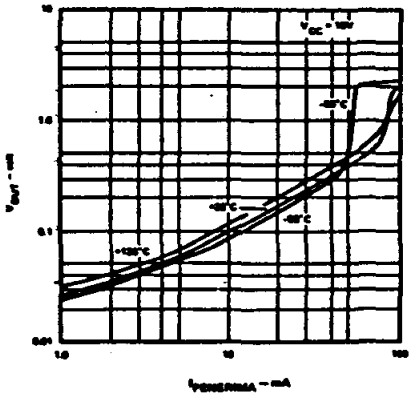
TEGANGAN KELUARAN TINGGI
vs. ARUS SUMBER KELUARAN



TEGANGAN KELUARAN RENDAH
vs. ARUS PENERIMA KELUARAN

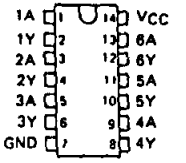


TEGANGAN KELUARAN RENDAH
vs. ARUS PENERIMA KELUARAN

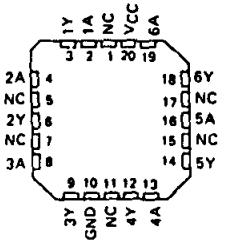


- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . N PACKAGE
SN74LS14 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

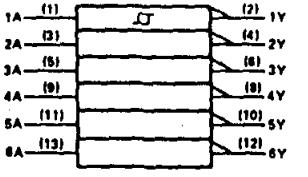
description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

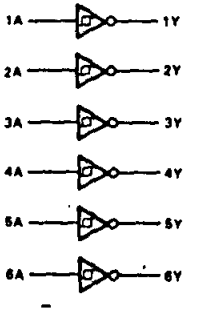
The SN5414 and SN54LS14 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7414 and the SN74LS14 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

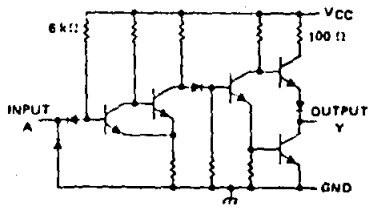


$Y = \overline{A}$

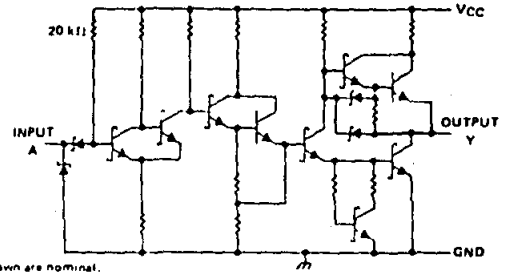
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

schematics

'14



'LS14



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '14 . . . . . 5.5 V
'LS14 . . . . . 7 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5414			SN7414			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			−0.8			−0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V_{T+}	V_{CC} = 5 V				1.5	1.7	2	V
V_{T-}	V_{CC} = 5 V				0.6	0.9	1.1	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V				0.4	0.8		V
V_{IK}	V_{CC} = MIN,	I_I = −12 mA					−1.5	V
V_{OH}	V_{CC} = MIN,	V_I = 0.8 V,	I_{OH} = −0.8 mA		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 2 V,	I_{OL} = 16 mA			0.2	0.4	V
I_{T+}	V_{CC} = 5 V,	$V_I = V_{T+}$				−0.43		mA
I_{T-}	V_{CC} = 5 V,	$V_I = V_{T-}$				−0.56		mA
I_I	V_{CC} = MAX,	V_I = 5.5 V					1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.4 V					40	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				−0.8	−1.2	mA
I_{OS}§	V_{CC} = MAX				−18		−55	mA
I_{CCH}	V_{CC} = MAX					22	36	mA
I_{CCL}	V_{CC} = MAX					39	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω,	C_L = 15 pF		15	22	ns
t_{PHL}						15	22	ns

recommended operating conditions

	SN54LS14			SN74LS14			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

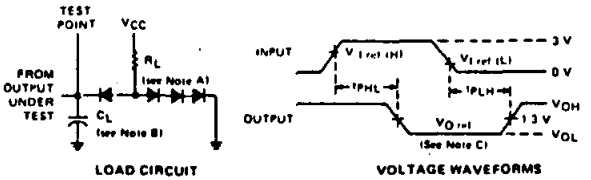
PARAMETER	TEST CONDITIONS†		SN54LS14			SN74LS14			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	V_{CC} = 5 V		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5 V		0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.8		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_I = 0.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_I = 1.9 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}			−0.14			−0.14		mA
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}			−0.18			−0.18		mA
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX			8.6	16		8.6	16	mA
I_{CCL}	V_{CC} = MAX			12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT — VOLTAGE WAVEFORMS

NOTES A. All diodes are 1N3064 or equivalent.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltage are

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\,ref(H)}$	$V_{I\,ref(L)}$	$V_{O\,ref}$
SN54'/SN74'	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

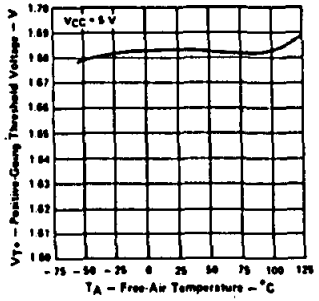


FIGURE 1

NEGATIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

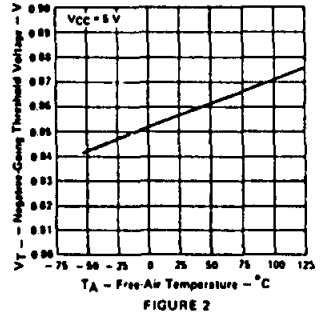


FIGURE 2

HYSTERESIS vs FREE-AIR TEMPERATURE

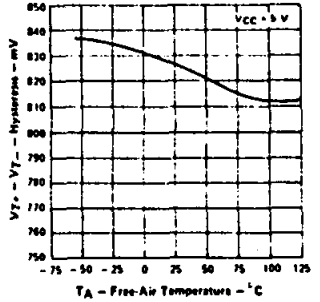


FIGURE 3

Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5414 only.

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

DISTRIBUTION OF UNITS FOR HYSTERESIS

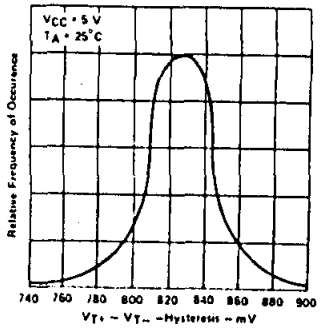


FIGURE 4

THRESHOLD VOLTAGES vs SUPPLY VOLTAGE

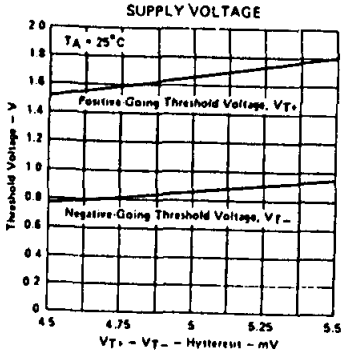


FIGURE 5

HYSTERESIS vs SUPPLY VOLTAGE

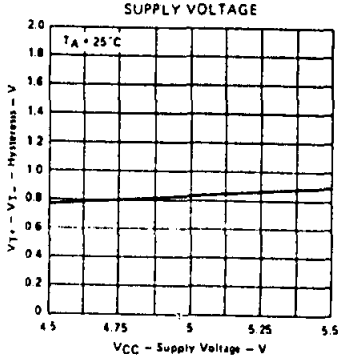


FIGURE 6

OUTPUT VOLTAGE vs INPUT VOLTAGE

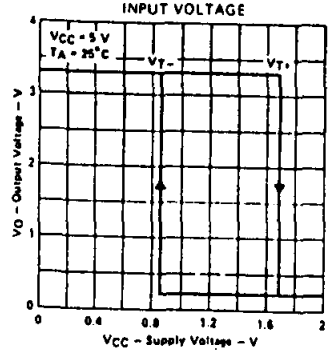


FIGURE 7

Data for temperatures below 0°C and 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN5414 only.

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

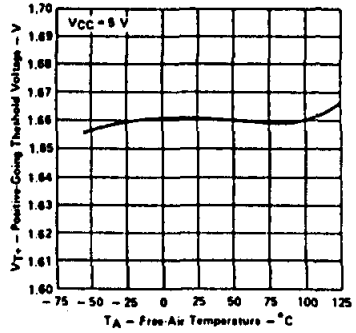


FIGURE 8

NEGATIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

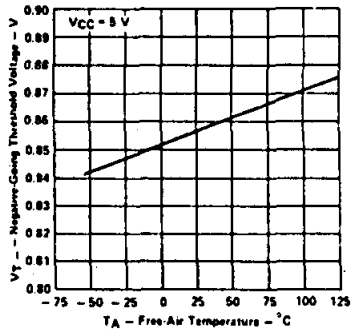


FIGURE 9

HYSTERESIS vs FREE-AIR TEMPERATURE

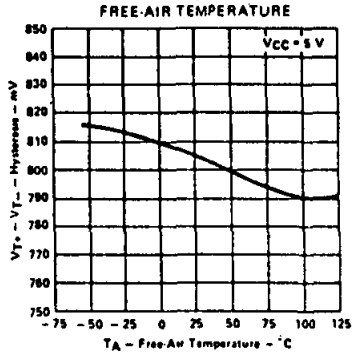


FIGURE 10

DISTRIBUTION OF UNITS FOR HYSTERESIS

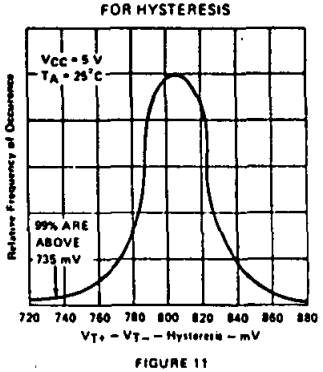


FIGURE 11

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

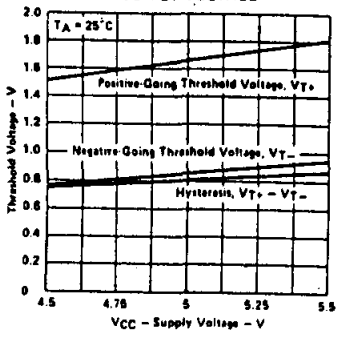


FIGURE 12

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

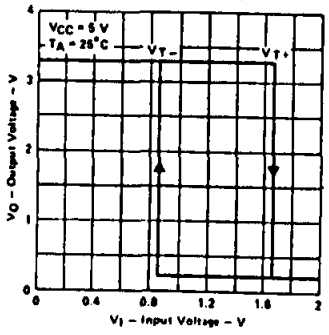
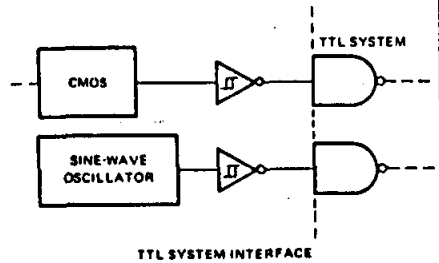


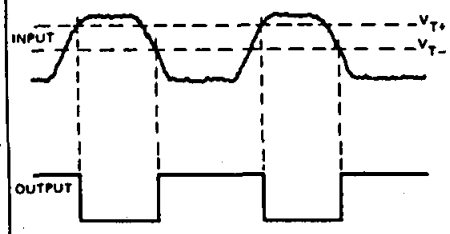
FIGURE 13

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

TYPICAL APPLICATION DATA

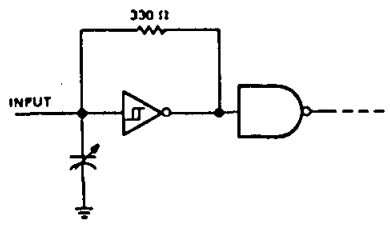


TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS

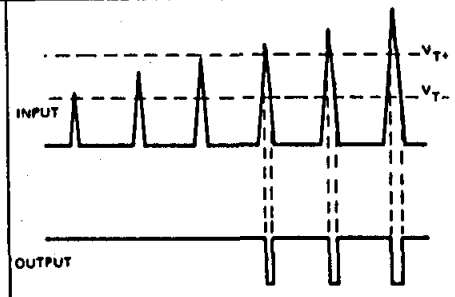


PULSE SHAPER

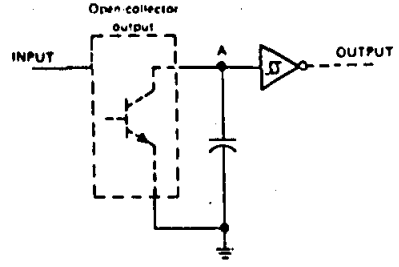
0.1 Hz to 10 MHz

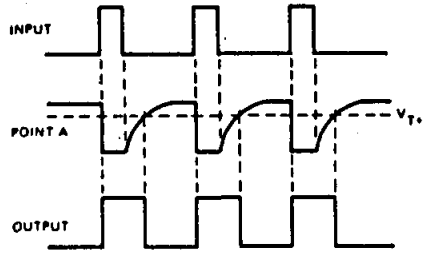


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

National Semiconductor Corporation

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

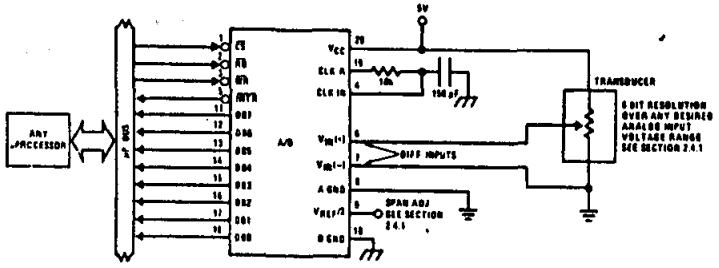
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

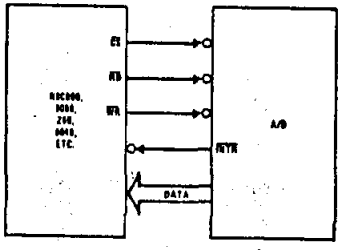
Resolution	8 bits
Total error	± ¼ LSB, ± ½ LSB and ± 1 LSB
Conversion time	100 μs

Typical Applications



TL/H/5671-1

8080 Interface



TL/H/5671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	± ¼ LSB		
ADC0802		± ½ LSB	
ADC0803	± ½ LSB		
ADC0804		± 1 LSB	
ADC0805			± 1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± ½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± 1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			± 1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		± 1/16	± ⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ± 10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		± 1/16	± ⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(WR)L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{CC}

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL *INPUTS* [*Note:* CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
$V_{OUT}(0)$	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	$I_{OUT} = 1.6\ mA$, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0\ mA$, $V_{CC} = 4.75\ V_{DC}$			0.4 0.4	V_{DC} V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640\ kHz$, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

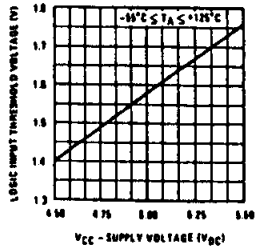
Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

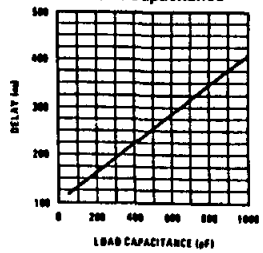
Note 9: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each resistor is 16k. Total ladder input resistance is the sum of the two equal resistors.

Typical Performance Characteristics

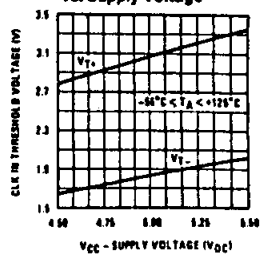
Logic Input Threshold Voltage vs. Supply Voltage



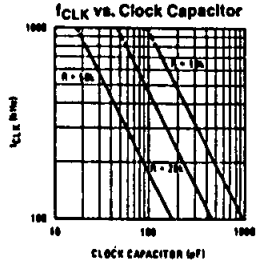
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



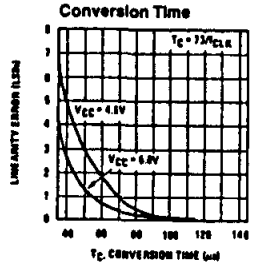
CLK IN Schmitt Trip Levels vs. Supply Voltage



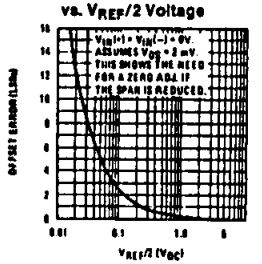
f_{CLK} vs. Clock Capacitor



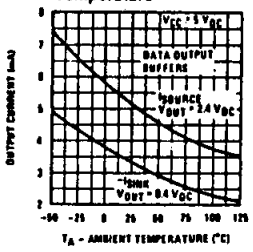
Full-Scale Error vs Conversion Time



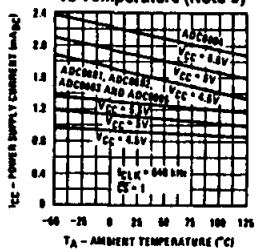
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



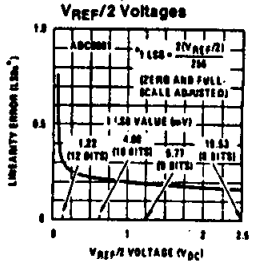
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



TL/H/5671–2

GENERAL DESCRIPTION

8192-word × 8-bit UV Erasable and Programmable Read Only Memory

The 2764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

FEATURES

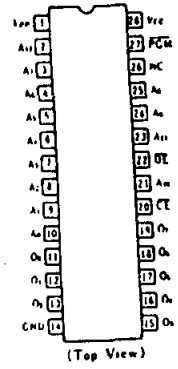
- Single Power Supply ..... +5V ± 5%
- Simple Programming Program Voltage: +21 V D.C.
  Program with one 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time ..... HN482764G-2 200ns max
  HN482764G 250ns max
  HN482764G-3* 300ns max
- High Performance Programming Available
- Low Standby current ..... 35mA max.

MODE SELECTION

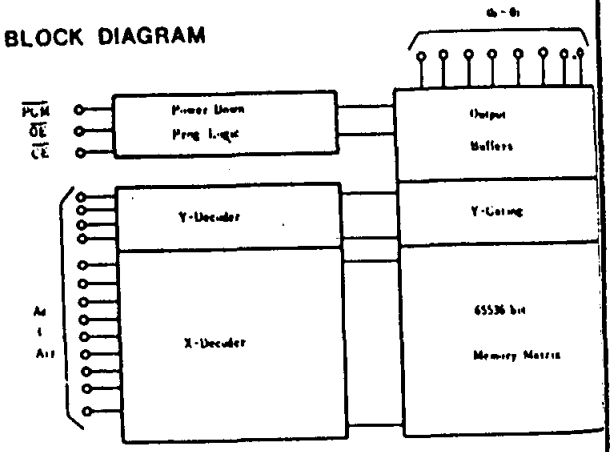
Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x = don't care

PIN CONNECTION



BLOCK DIAGRAM



GENERAL DESCRIPTION

16384-word × 8-bit UV Erasable and Programmable Read Only Memory

The 27128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can be written into the device.

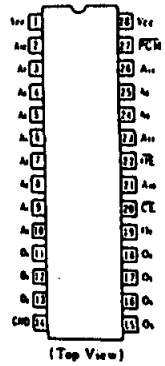
FEATURES

- Single Power supply ..... +5V ± 5%
- Simple Programming Program Voltage: +21 V DC
  Program with One 50ms Pulse
- Static ..... No Clocks Required
  Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 250ns/300ns/450ns
- Absolute Max. Rating of V_{PP} Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available

MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

PIN CONNECTION



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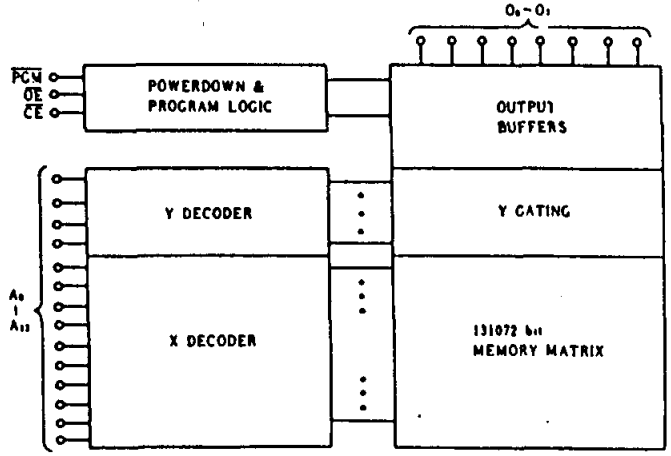
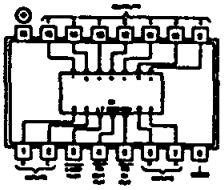


46, 246 Penggerak/dekoder BCD-7-segmen dengan jalankeluar kolektor terbuka (30 V)

47, 247 dengan jalankeluar kolektor terbuka (15 V)

347, 447 dengan jalankeluar kolektor terbuka (7 V)



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS (6= 6 and 9= 9 for 246, 247, LS247 and LS447)

Decimal or Function	Inputs LT	RBI	D	C	B	A	BI/RBO†	Outputs a	b	c	d	e	f	g	note
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

Function table
• 46A, 47A, LS47, LS347
• 246, 247, LS247, LS447

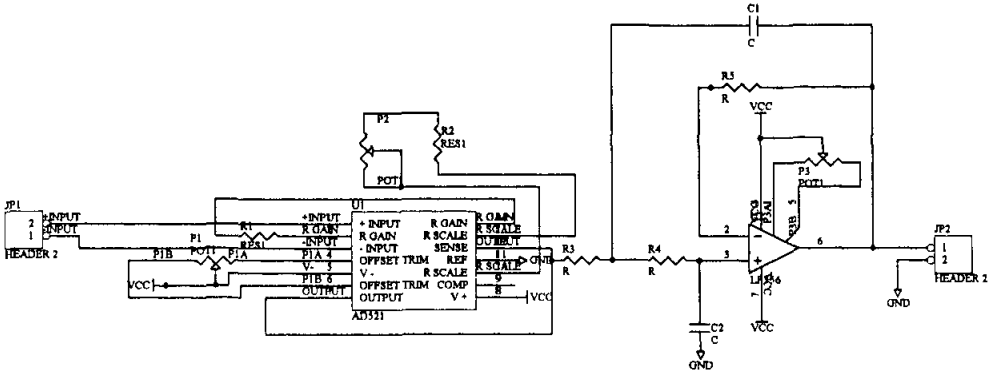
CATATAN:

1. Jalanmasuk polosan ($\overline{BI}$) harus terbuka atau ditaruh pada taraf logika tinggi bila fungsi-fungsi keluaran 0 hingga 15 diinginkan. Jalanmasuk polosan deret ($\overline{RBI}$) harus terbuka atau tinggi kalau pemolosan nol dasan tidak diinginkan.
2. Kalau taraf logika rendah dikenakan dengan langsung kepada jalanmasuk polosan ($\overline{BI}$) maka semua jalankeluar segmen adalah off tak perduli akan taraf yang ada di sebarang jalanmasuk lain.
3. Bila jalanmasuk polosan deret ($\overline{RBI}$) dan juga jalanmasuk-jalanmasuk A, B, C, dan D berada dalam taraf rendah dengan *lamp test* tinggi, maka semua segmen keluaran off dan jalankeluar polosan deret ($\overline{RBO}$) pergi ke taraf rendah (kondisi tanggap).
4. Kalau jalanmasuk polosan/jalankeluar polosan deret ($\overline{BI}/\overline{RBO}$) terbuka atau dibiarkan tinggi, dan jalanmasuk *lamp test* dibuat rendah, maka semua segmen keluaran adalah on.

† $\overline{BI}/\overline{RBO}$ adalah logika AND kawat yang berguna sebagai jalanmasuk polosan ($\overline{BI}$) dan/atau jalankeluar polosan deret ($\overline{RBO}$)

	supply curr. (mA)	t_{PLH} (ns)	t_{PHL} (ns)
46A 47A 246 247	64	100	100
LS47 LS247 LS347 LS447	7	100	100

		Condition	Fan-in	Fan-out
46A 47A 246 247	$\overline{BI}/\overline{RBO}$ inp.	L	2,5	
		H	1	
	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L/H		6
	other outp.	L		25
LS47 LS247	$\overline{BI}/\overline{RBO}$ inp.	L	3	
		H	1	
	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L		6
		H		2,5
	other outp.	L		60
LS347 LS447	$\overline{BI}/\overline{RBO}$ inp.	L	3	
		H	1	
	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L		6
		H		2,5
	other outp.	L		60



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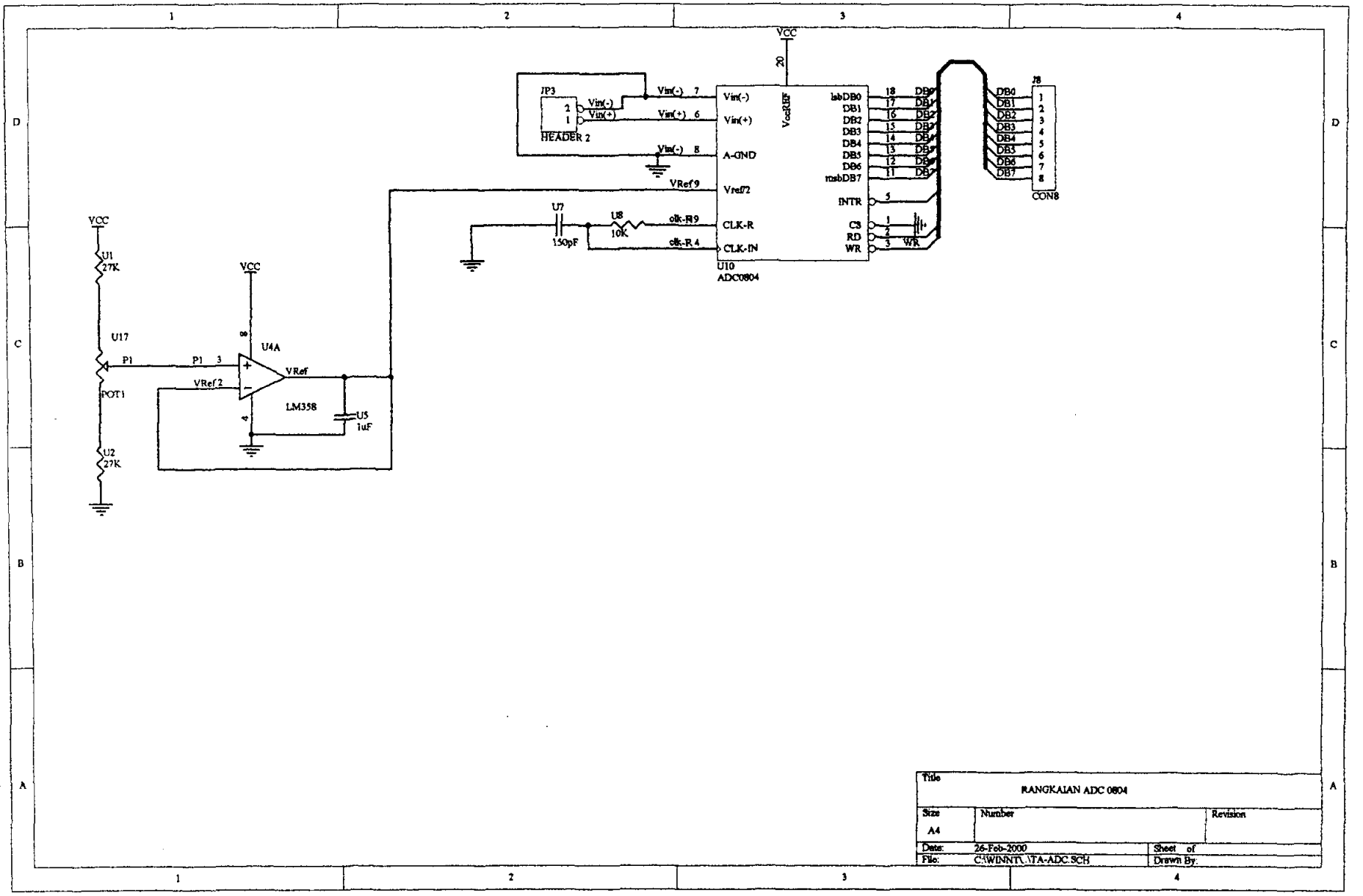
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U1
27K
U17
P1
POT1
U2
27K
VCC
U4A
P1 3
VRef2
VRef
LM358
U5
1uF
JP3
Vin(-)
Vin(+)
HEADER 2
Vin(-) 7
Vin(+) 6
Vin(-) 8
VRef/2
U7
150pF
U8
10K
clk-R9
clk-R4
Vin(-)
Vin(+)
A-GND
Vref/2
CLK-R
CLK-IN
U10
ADC0804
20
VccREF
labDB0
DB1
DB2
DB3
DB4
DB5
DB6
rssbDB7
INTR
CS
RD
WR
18
17
16
15
14
13
12
11
5
1
2
3
WR
J8
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
1
2
3
4
5
6
7
8
CON8
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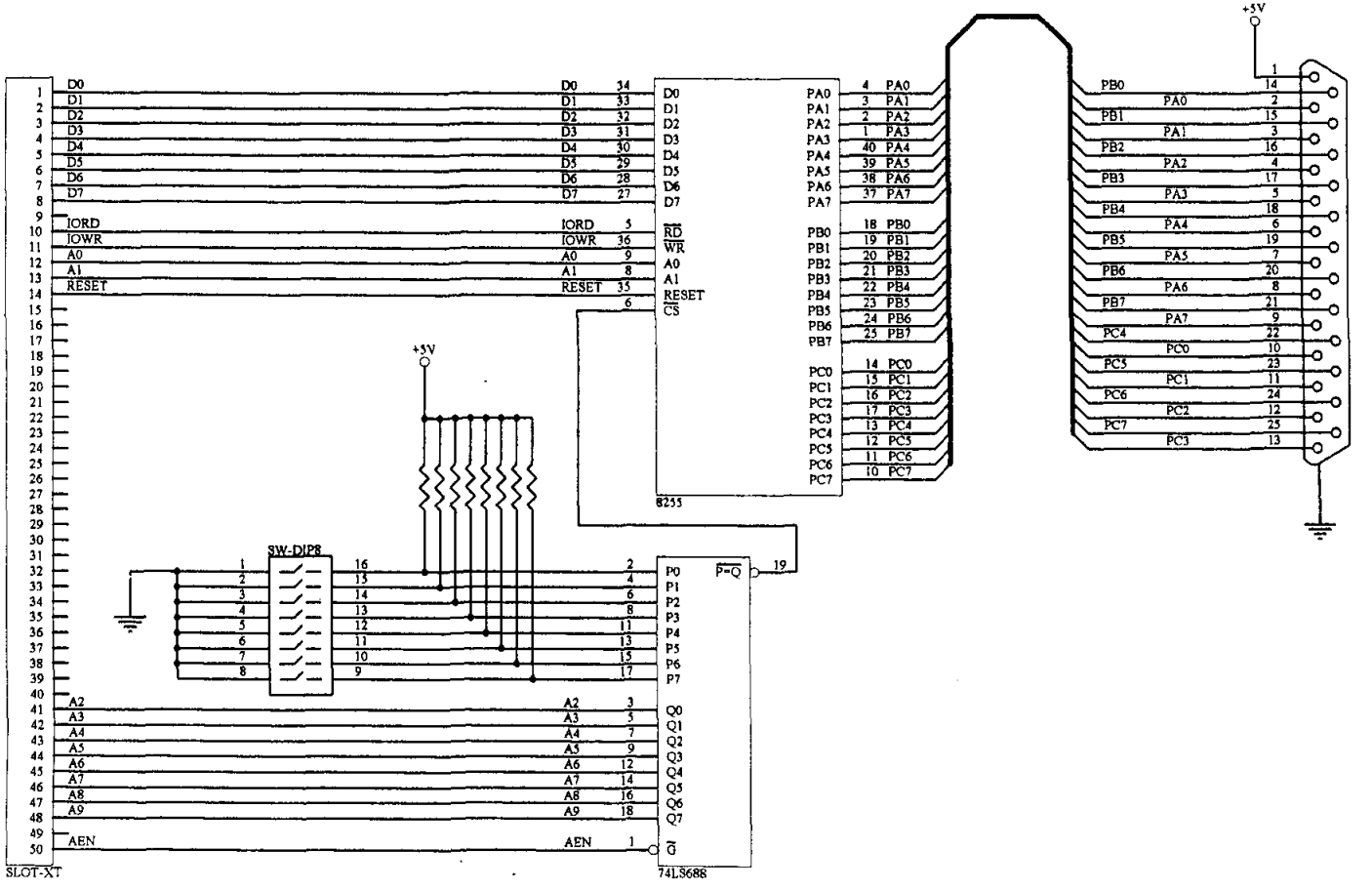

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BIODATA

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NIRM	: 95.7.003.31073.51924
Tempat, Tanggal Lahir	: Surabaya, 9 April 1977
Agama	: Kristen
Alamat	: Jl. Rungkut Menanggal Harapan W /19, Surabaya.

Riwayat Pendidikan:

- Tahun 1989 Lulus SDK Petra 9 Surabaya.
- Tahun 1992 Lulus SMPK Petra 5 Surabaya.
- Tahun 1995 Lulus SMAK Petra 5 Surabaya.
- Tahun 2000 Lulus Sarjana Fakultas Teknik Jurusan Teknik Elektro Universitas Katolik Widya Mandala Surabaya.