LAMPIRAN

```
{Oleh : BUDI (Nrp : 5103094043)}

uses newdelay,crt,dos;

const dac=$300;
      adc=$302;
      fcb=$58;
      fs=10000;
      sampel=1024;

var y,h,hd,w,h1,h2                   : array[0..sampel] of real;
    x                                : array[0..sampel] of integer;
    i,j,l,k,n,k1                     : integer;
    yd,fc,fc1,fc2,sa,tw,fc_up,fc_down : real;
    menu                             : char;

{Abstrak : procedure Lpf adalah prosedur untuk Lowpass Filter yang
didalamnya berisi penetapan harga input untuk frekuensi cutoff,
transition width, dan stopband attenuation serta perhitungan
koefisien filter}
procedure Lpf;
begin
     repeat
     clrscr;
     writeln('=================');
     writeln(' LOWPASS FILTER ');
     writeln('=================');
     writeln;
     write('Frek. cutoff (Hz)        = ');readln(fc1);
     write('Transition Width (Hz)    = ');readln(tw);
     write('Stopband Attenuation (dB) = ');readln(sa);
     if sa<=21 then
        begin
        writeln('Window                  = Rectangular');
        fc:=fc1/(fs+15000);
        k:=round(0.9*(fs+15000)/tw);
        writeln('Jumlah koefisien filter  = ',k);
        if k>100 then writeln('Filter tidak mampu !!!');
        delay(1000);
        for n:=0 to (k-1) do
         begin
         if n=0 then h[0]:=2*fc
         else h[n]:=(2*fc*sin(n*2*pi*fc))/(n*2*pi*fc);
         end;
        end;
      if (sa>21) and (sa<=53) then
         begin
         writeln('Window                  = Hamming');
         fc:=fc1/(fs+5000);
         k:=round(3.3*(fs+5000)/tw);
         writeln('Jumlah koefisien filter  = ',k);
         if k>100 then writeln('Filter tidak mampu !!!');
         delay(1000);
```

```pascal
         for n:=0 to (k-1) do
         begin
         if n=0 then h[0]:=2*fc
         else hd[n]:=(2*fc*sin(n*2*pi*fc))/(n*2*pi*fc);
         if n=0 then w[0]:=1
         else w[n]:=0.54+0.46*cos((2*pi*n)/k);
         h[n]:=hd[n]*w[n]*1.25;
         end;
      end;
    if (sa>53) and (sa<=74) then
      begin
      writeln('Window                   = Blackman');
      fc:=fc1/(fs+2000);
      k:=round(5.5*(fs+2000)/tw);
      writeln('Jumlah koefisien filter    = ',k);
      if k>100 then writeln('Filter tidak mampu !!!');
      delay(1000);
      for n:=0 to (k-1) do
       begin
       if n=0 then h[0]:=2*fc
       else hd[n]:=(2*fc*sin(n*2*pi*fc))/(n*2*pi*fc);
       if n=0 then w[0]:=1
       else
     w[n]:=0.42+0.5*cos((2*pi*n)/(k-1))+0.08*cos((4*pi*n)/(k-1));
       h[n]:=hd[n]*w[n]*1.25;
       end;
      end;
    until (k<=100);
end;

{Abstrak : procedure Bpf adalah prosedur untuk Bandpass Filter
yang didalamnya berisi penetapan harga input untuk frekuensi
cutoff atas dan bawah, transition width, dan stopband attenuation
serta perhitungan koefisien filter}
procedure Bpf;
begin
    repeat
    clrscr;
    writeln('==================');
    writeln(' BANDPASS FILTER ');
    writeln('==================');
    writeln;
    write('fc atas (Hz)             = ');readln(fc_up);
    write('fc bawah (Hz)            = ');readln(fc_down);
    write('Transition Width (Hz)    = ');readln(tw);
    write('Stopband Attenuation (dB) = ');readln(sa);
    if sa<=21 then
        begin
        writeln('Window                   = Rectangular');
        fc2:=(fc_up)/(fs+10000);
        fc1:=(fc_down)/(fs+10000);
        k:=round(0.9*(fs+10000)/tw);
        writeln('Jumlah koefisien filter    = ',k);
        if k>100 then writeln('Filter tidak mampu !!!');
        delay(1000);
```

```pascal
      for n:=0 to (k-1) do
      begin
      if n=0 then h[0]:=2*(fc2-fc1)
      else begin
           h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
           h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
           h[n]:=(h2[n]-h1[n]);
           end;
      end;
    end;
  if (sa>21) and (sa<=53) then
     begin
     writeln('Window                    = Hamming');
     fc2:=(fc_up)/(fs+4000);
     fc1:=(fc_down)/(fs+4000);
     k:=round(3.3*(fs+4000)/tw);
     writeln('Jumlah koefisien filter   = ',k);
     if k>100 then writeln('Filter tidak mampu !!!');
     delay(1000);
     for n:=0 to (k-1) do
      begin
      if n=0 then h[0]:=2*(fc2-fc1)
      else begin
           h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
           h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
           if n=0 then w[0]:=1
           else w[n]:=0.54+0.46*cos((2*pi*n)/k);
           h[n]:=(h2[n]-h1[n])*w[n];
           end;
      end;
    end;
  if (sa>53) and (sa<=74) then
     begin
     writeln('Window                    = Blackman');
     fc2:=(fc_up)/(fs+2500);
     fc1:=(fc_down)/(fs+2500);
     k:=round(5.5*(fs+2500)/tw);
     writeln('Jumlah koefisien filter   = ',k);
     if k>100 then writeln('Filter tidak mampu !!!');
     delay(1000);
     for n:=0 to (k-1) do
      begin
      if n=0 then h[0]:=2*(fc2-fc1)
      else begin
           h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
           h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
           if n=0 then w[0]:=1
           else
  w[n]:=0.42+0.5*cos((2*pi*n)/(k-1))+0.08*cos((4*pi*n)/(k-1));
           h[n]:=(h2[n]-h1[n])*w[n];
           end;
      end;
    end;
until (k<=100);
end;
```

```
{Abstrak : procedure Bsf adalah prosedur untuk Bandstop Filter
yang didalamnya berisi penetapan harga input untuk frekuensi
cutoff atas dan bawah, transition width, dan stopband attenuation
serta perhitungan koefisien filter}
procedure Bsf;
begin
     repeat
     clrscr;
     writeln('=================');
     writeln(' BANDSTOP FILTER ');
     writeln('=================');
     writeln;
     write('fc atas (Hz)             = ');readln(fc_up);
     write('fc bawah (Hz)            = ');readln(fc_down);
     write('Transition Width (Hz)    = ');readln(tw);
     write('Stopband Attenuation (dB) = ');readln(sa);
     if sa<=21 then
         begin
         writeln('Window                 = Rectangular');
         fc2:=fc_up/(fs+10000);
         fc1:=fc_down/(fs+10000);
         k:=round(0.9*(fs+10000)/tw);
         writeln('Jumlah koefisien filter  = ',k);
         if k>100 then writeln('Filter tidak mampu !!!');
         delay(1000);
         for n:=0 to (k-1) do
          begin
          if n=0 then h[0]:=1-2*(fc2-fc1)
          else begin
               h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
               h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
               h[n]:=h1[n]-h2[n];
               end;
          end;
         end;
     if (sa>21) and (sa<=53) then
         begin
         writeln('Window                 = Hamming');
         fc2:=fc_up/(fs+2000);
         fc1:=fc_down/(fs+2000);
         k:=round(3.3*(fs+2000)/tw);
         writeln('Jumlah koefisien filter  = ',k);
         if k>100 then writeln('Filter tidak mampu !!!');
         delay(1000);
         for n:=0 to (k-1) do
          begin
          if n=0 then h[0]:=1-2*(fc2-fc1)
          else begin
               h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
               h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
               if n=0 then w[0]:=1
               else begin w[n]:=0.54+0.46*cos((2*pi*n)/k);
               h[n]:=(h1[n]-h2[n])*w[n]; end;
               end;
          end;
         end;
```

```pascal
    if (sa>53) and (sa<=74) then
       begin
       writeln('Window                        = Blackman');
       fc2:=fc_up/fs;
       fc1:=fc_down/fs;
       k:=round(5.5*fs/tw);
       writeln('Jumlah koefisien filter    = ',k);
       if k>100 then writeln('Filter tidak mampu !!!');
       delay(1000);
       for n:=0 to (k-1) do
        begin
        if n=0 then h[0]:=1-2*(fc2-fc1)
        else begin
            h2[n]:=(2*fc2*sin(n*2*pi*fc2))/(n*2*pi*fc2);
            h1[n]:=(2*fc1*sin(n*2*pi*fc1))/(n*2*pi*fc1);
            if n=0 then w[0]:=1
            else begin
      w[n]:=0.42+0.5*cos((2*pi*n)/(k-1))+0.08*cos((4*pi*n)/(k-1));
            h[n]:=(h1[n]-h2[n])*w[n]; end;
            end;
        end;
       end;
    until (k<=100);
end;

{Abstrak  :  procedure  interrupt  untuk  Baca_ADC  dan  Baca_ADC1
berfungsi untuk pengaturan pengambilan data/sampel dan tap filter,
pengolahan dan perhitungan output Filter Digital}
procedure Baca_ADC; interrupt;
begin
    x[i]:=portw[adc] and $FFF;            {baca data pada adc}
    x[i]:=x[i] xor $800;
    yd:=0;
    for l:=0 to 31 do
        begin
        j:=i-1;
        if j<0 then j:=sampel+j;
        yd:=yd+((h[l]*x[j]));
        end;
    portw[adc]:=fcb;
    y[i]:=yd;
    portw[dac]:=round(y[i]);
    inc(i);
    if i>=sampel then i:=0;
    port[$20]:=$20;        {normal end of interrupt PIC 8259 slave}
end;
procedure Baca_ADC1; interrupt;
begin
    x[i]:=portw[adc] and $FFF;            {baca data pada adc}
    x[i]:=x[i] xor $800;
    yd:=0;
    k1:=k-1;
    for l:=0 to k1 do
        begin
        j:=i-1;
        if j<0 then j:=sampel+j;
```

```pascal
            yd:=yd+((h[l]*x[j]));
        end;
    portw[adc]:=fcb;
    y[i]:=yd;
    if y[i]>2048 then portw[dac]:=round(y[i])-2048
    else if y[i]<2048 then portw[dac]:=round(y[i])+2048
    else portw[dac]:=round(y[i]);
    inc(i);
    if i>=sampel then i:=0;
    port[$20]:=$20;         {normal end of interrupt PIC 8259 slave}
end;


{Abstrak : Program Utama berisi tentang inisialisasi ADC, tampilan
menu filter, pengaturan set interrupt vector untuk procedure
interrupt Baca_ADC dan Baca_ADC1, dan IRQ}

{Program Utama}
begin
clrscr;
    portw[adc]:=fcb;                        {inisialisasi ADC}
    i:=0;
    writeln('=================');
    writeln('  FILTER DIGITAL ');
    writeln('=================');
    writeln('1. LOWPASS FILTER');
    writeln('2. BANDPASS FILTER');
    writeln('3. BANDSTOP FILTER');
    writeln('=================');
    write('Type Filter yang dipilih : ');readln(menu);
    case menu of
    '1' : Lpf;
    '2' : Bpf;
    '3' : Bsf;
    end;
    if (menu='1') or (menu='3') then
    SetIntVec($0D,Addr(Baca_ADC));
    if menu='2' then SetIntVec($0D,Addr(Baca_ADC1));
    port[$21]:=port[$21] and $DF;        {enable IRQ5}
    repeat
    until keypressed;
    port[$21]:=port[$21] or $20;         {disable IRQ5}
end.
```

Lampiran 2 : Gambar Rangkaian Skematik Alat

Title	INTERFACING ADC - DAC	
Size	Number	Revision
B		
Date:	23-Mar-2000	Sheet of
File:	C:\BI-DI\BUDI\ASKEMA.SCH	Drawn By: BUDI (8103094843)
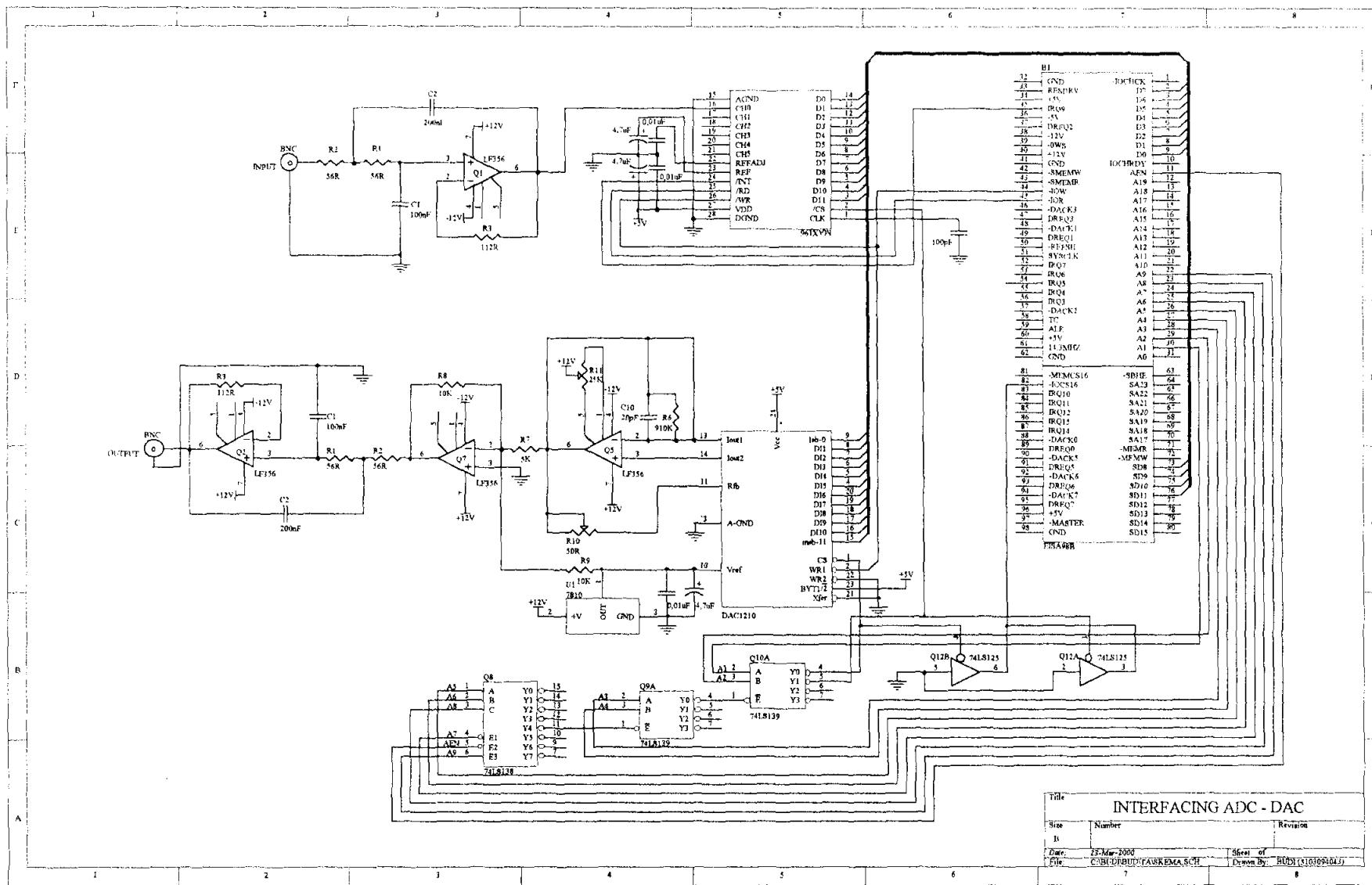
19 0435; Rev 0; 9/95

EVALUATION KIT AVAILABLE

///XI///
Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

MAX196/MAX198

General Description

The MAX196/MAX198 multirange, 12-bit data-acquisition systems (DAS) require only a single +5V supply for operation, yet convert analog signals at their inputs up to ±10V (MAX196) and ±4V (MAX198). These systems provide six analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0V to +10V, and 0V to +5V for the MAX196; ±VREF, ±VREF/2, 0V to +VREF, and 0V to +VREF/2 for the MAX198. This range switching increases the effective dynamic range to 14 bits and provides the flexibility to interface ±12V, ±15V, and 4mA to 20mA powered sensors to a single +5V system. In addition, these converters are fault protected to ±16.5V; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, 100ksps throughput rate, software-selectable internal/external clock, internal/external acquisition control, 12-bit parallel interface, and internal 4.096V or external reference.

Two programmable power-down modes (STBYPD, FULLPD) provide low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX196/MAX198 employ a standard microprocessor (µP) interface. A three-state data I/O port is configured to operate with 16-bit data buses, and data-access and bus-release timing specifications are compatible with most popular µPs. All logic inputs and outputs are TTL/CMOS compatible.

These devices are available in 28-pin DIP, wide SO, SSOP (55% smaller in area than wide SO), and ceramic SB packages. For 8+4 bus interface, see the MAX197 and the MAX199 data sheets. An evaluation kit will be available after December 1995 (MAX196EVKIT-DIP).

Applications

Industrial-Control Systems

Robotics

Data-Acquisition Systems

Automatic Testing Systems

Medical Instruments

Telecommunications

Functional Diagram appears at end of data sheet.

Features

♦ 12-Bit Resolution, 1/2LSB Linearity
♦ Single +5V Supply Operation
♦ Software-Selectable Input Ranges:
  ±10V, ±5V, 0V to +10V, 0V to +5V (MAX196)
  ±VREF, ±VREF/2, 0V to +VREF, 0V to +VREF/2 (MAX198)
♦ Internal 4.096V or External Reference
♦ Fault-Protected Input Multiplexer
♦ 6 Analog Input Channels
♦ 6µs Conversion Time, 100ksps Sampling Rate
♦ Internal or External Acquisition Control
♦ Two Power-Down Modes
♦ Internal or External Clock

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX196ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX196BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX196ACWI	0°C to +70°C	28 Wide SO
MAX196BCWI	0°C to +70°C	28 Wide SO
MAX196ACAI	0°C to +70°C	28 SSOP
MAX196BCAI	0°C to +70°C	28 SSOP

Ordering Information continued at end of data sheet.

Pin Configuration

TOP VIEW

CLK	1	28 DGND
$\overline{CS}$	2	27 VDD
D11	3	26 $\overline{WR}$
D10	4	25 $\overline{RD}$
D9	5	24 $\overline{INT}$
D8	6	23 REF
D7	7	22 REFADJ
D6	8	21 CH5
D5	9	20 CH4
D4	10	19 CH3
D3	11	18 CH2
D2	12	17 CH1
D1	13	16 CH0
D0	14	15 AGND

///XI/// MAX196 MAX198

DIP/SO/SSOP/Ceramic SB
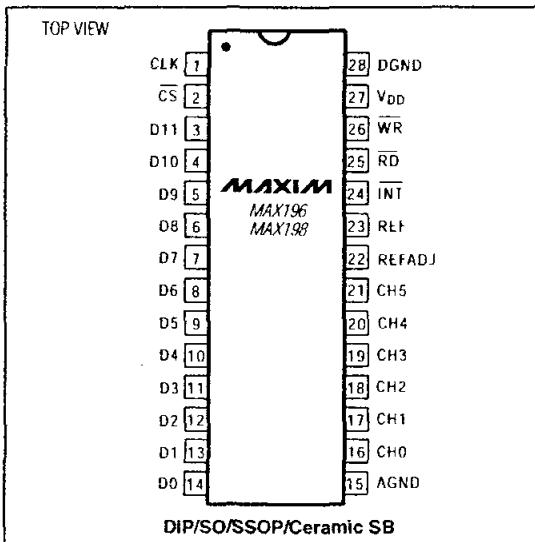
///XI/// ———————————————————————— *Maxim Integrated Products* 1

Call toll free 1-800-722-8266 for free samples or literature.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	-0.3V to +7V
AGND to DGND	-0.3V to +0.3V
REF to AGND	-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND	-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND	-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND	-0.3V to (V_{DD} + 0.3V)
CH0–CH5 to AGND	±16.5V
Continuous Power Dissipation ($T_A = +70°C$)	
Narrow Plastic DIP (derate 14.29mW/°C above +70°C)	1143mW

Wide SO (derate 12.50mW/°C above +70°C)	1000mW
SSOP (derate 9.52mW/°C above +70°C)	762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)	1600mW
Operating Temperature Ranges	
MAX196_C_I/MAX198_C_I	0°C to +70°C
MAX196_E_I/MAX198_E_I	-40°C to +85°C
MAX196_MYI/MAX198_MYI	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted. Typical values are at $T_A = +25°C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX196A/MAX198A				±1/2	LSB
		MAX196B/MAX198B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX196A/MAX198A			±3	LSB
			MAX196B/MAX198B			±5	
		Bipolar	MAX196A/MAX198A			±5	
			MAX196B/MAX198B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.5		
Gain Error (Note 2)		Unipolar	MAX196A/MAX198A			±7	LSB
			MAX196B/MAX198B			±10	
		Bipolar	MAX196A/MAX198A			±7	
			MAX196B/MAX198B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar			3		ppm/°C
		Bipolar			5		
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10Vp-p (MAX196) or ±4.096Vp-p (MAX198), f_{SAMPLE} = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD	MAX196A/MAX198A		70			dB
		MAX196B/MAX198B		69			
Total Harmonic Distortion	THD	Up to the 5th harmonic			-85	-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz, $V_{IN} = ±5V$ (MAX196) or ±4V (MAX198) (Note 3)			-86		dB
Aperture Delay		External CLK mode/external acquisition control			15		ns
Aperture Jitter		External CLK mode/external acquisition control			<50		ps
		Internal CLK mode/internal acquisition control (Note 4)			10		ns

MAXIM

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

(V$_{DD}$ = 5V ±5%; unipolar/bipolar range; external reference mode, V$_{REF}$ = 4.096V; 4.7µF at REF pin; external clock, f$_{CLK}$ = 2.0MHz with 50% duty cycle; T$_A$ = T$_{MIN}$ to T$_{MAX}$; unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG INPUT								
Track/Hold Acquisition Time		f$_{CLK}$ = 2.0MHz					3	µs
Small-Signal Bandwidth		-3dB rolloff	±10V or ±V$_{REF}$ range			5		MHz
			±5V or ±V$_{REF}$/2 range			2.5		
			0V to 10V or 0V to V$_{REF}$ range			2.5		
			0V to 5V or 0V to V$_{REF}$/2 range			1.25		
Input Voltage Range (see Table 3)	V$_{IN}$	Unipolar	MAX196		0		10	V
					0		5	
			MAX198		0		V$_{REF}$	
					0		V$_{REF}$/2	
		Bipolar	MAX196		-10		10	
					-5		5	
			MAX198		-V$_{REF}$		V$_{REF}$	
					-V$_{REF}$/2		V$_{REF}$/2	
Input Current	I$_{IN}$	Unipolar	MAX196	0V to 10V range			720	µA
				0V to 5V range			360	
			MAX198			0.1	10	
		Bipolar	MAX196	±10V range	-1200		720	
				±5V range	-600		360	
			MAX198	±V$_{REF}$ range	-1200		10	
				±V$_{REF}$/2 range	-600		10	
Input Resistance	ΔV$_{IN}$ / ΔI$_{IN}$	Unipolar				21		kΩ
		Bipolar				16		
Input Capacitance		(Note 5)					40	pF
INTERNAL REFERENCE								
REF Output Voltage	V$_{REF}$	T$_A$ = +25°C			4.076	4.096	4.116	V
REF Output Tempco (Contact Maxim Applications for guaranteed temperature drift specifications)	TC V$_{REF}$	MAX196_C/MAX198_C				15		ppm/°C
		MAX196_E/MAX198_E				30		
		MAX196_M/MAX198_M				40		
Output Short-Circuit Current							30	mA
Load Regulation		0mA to 0.5mA output current (Note 6)					10	mV
Capacitive Bypass at REF					4.7			µF
REFADJ Output Voltage					2.465	2.500	2.535	V
REFADJ Adjustment Range		With recommended circuit (Figure 1)				±1.5		%
Buffer Voltage Gain						1.6384		V/V

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7μF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT (buffer disabled, reference input applied to REF pin)							
Input Voltage Range				2.4		4.18	V
Input Current		V_{REF} = 4.18V	Normal, or STANDBY power-down mode			400	μA
			FULL power-down mode			1	
Input Resistance		Normal, or STANDBY power-down mode		10			kΩ
		FULL power-down mode		5			MΩ
REFADJ Threshold for Buffer Disable					V_{DD} - 50mV		V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		STANDBY power-down mode			700	850	μA
		FULL power-down mode (Note 7)			60	120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference - 4.096V			±0.1	±1/2	LSB
		Internal reference			±1/2		
TIMING							
Internal Clock Frequency	f_{CLK}	C_{CLK} = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	f_{CLK}			0.1		2.0	MHz
Acquisition Time	t_{ACQI}	Internal acquisition	External CLK	3.0			μs
			Internal CLK	3.0		5.0	
	t_{ACQE}	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	t_{CONV}	External CLK		6.0			μs
		Internal CLK, C_{CLK} = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, C_{CLK} = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		μs
Reference Buffer Settling		To 0.1mV REF bypass capacitor fully discharged	C_{REF} = 4.7μF		8		ms
			C_{REF} = 33μF		60		
DIGITAL INPUTS (D7–D0, CLK, RD, WR, CS) (Note 11)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				±10	μA
Input Capacitance	C_{IN}	(Note 5)				15	pF

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ELECTRICAL CHARACTERISTICS (continued)

(V$_{DD}$ = 5V ±5%; unipolar/bipolar range; external reference mode, V$_{REF}$ = 4.096V; 4.7µF at REF pin; external clock, f$_{CLK}$ = 2.0MHz with 50% duty cycle; T$_A$ = T$_{MIN}$ to T$_{MAX}$; unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D11–D0, INT)						
Output Low Voltage	V$_{OL}$	V$_{DD}$ = 4.75V, I$_{SINK}$ = 1.6mA			0.4	V
Output High Voltage	V$_{OH}$	V$_{DD}$ = 4.75V, I$_{SOURCE}$ = 1mA	V$_{DD}$ - 1			V
Three-State Output Capacitance	C$_{OUT}$	(Note 5)			15	pF

TIMING CHARACTERISTICS

(V$_{DD}$ = 5V ±5%; unipolar/bipolar range; external reference mode, V$_{REF}$ = 4.096V; 4.7µF at REF pin; external clock, f$_{CLK}$ = 2.0MHz with 50% duty cycle; T$_A$ = T$_{MIN}$ to T$_{MAX}$; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS Pulse Width	t$_{CS}$		80			ns
WR Pulse Width	t$_{WR}$		80			ns
CS to WR Setup Time	t$_{CSWS}$		0			ns
CS to WR Hold Time	t$_{CSWH}$		0			ns
CS to RD Setup Time	t$_{CSRS}$		0			ns
CS to RD Hold Time	t$_{CSRH}$		0			ns
CLK to WR Setup Time	t$_{CWS}$				100	ns
CLK to WR Hold Time	t$_{CWH}$				50	ns
Data Valid to WR Setup	t$_{DS}$		60			ns
Data Valid to WR Hold	t$_{DH}$		0			ns
RD Low to Output Data Valid	t$_{DO}$	Figure 2, C$_L$ = 100pF (Note 12)			120	ns
RD High to Output Disable	t$_{TR}$	(Note 13)			70	ns
RD Low to INT High Delay	t$_{INT1}$				120	ns

Note 1: Accuracy specifications tested at V$_{DD}$ = 5.0V. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the ±10V (MAX196) and ±4.096V (MAX198) input ranges.
Note 2: External reference: V$_{REF}$ = 4.096V; offset error nulled, ideal last code transition = FS - 3/2LSB.
Note 3: Ground "on" channel; sine wave applied to all "off" channels.
Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.
Note 5: Guaranteed by design. Not tested.
Note 6: Use static loads only.
Note 7: Tested using internal reference.
Note 8: PSRR measured at full-scale.
Note 9: External acquisition timing: starts at data valid at ACQMOD = low control byte; ends at rising edge of WR with ACQMOD = high control byte.
Note 10: Not subject to production testing. Provided for design guidance only.
**Note 11:** All input control signals specified with t$_R$ = t$_F$ = 5ns from a voltage level of 0.8V to 2.4V.
Note 12: t$_{DO}$ is measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 13: t$_{TR}$ is defined as the time required for the data lines to change by 0.5V.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

(T_A = +25°C, unless otherwise noted.)

INTEGRAL NONLINEARITY vs. DIGITAL CODE

FFT PLOT

EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY

REFERENCE OUTPUT VOLTAGE (V_REF) vs. TEMPERATURE

POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE

CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE

CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE

MAXIM
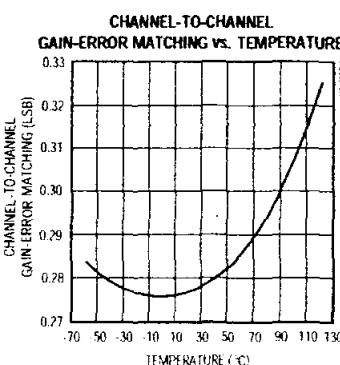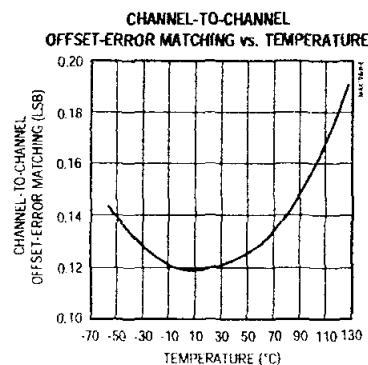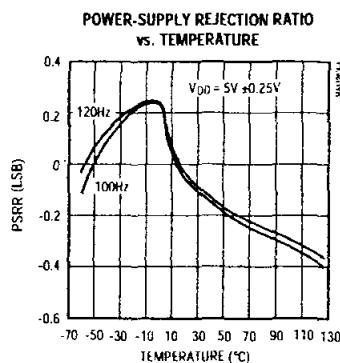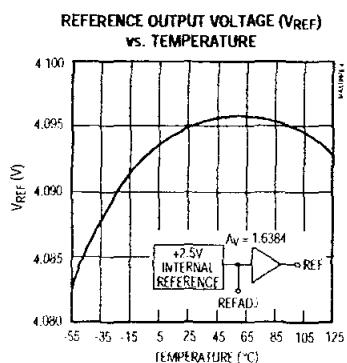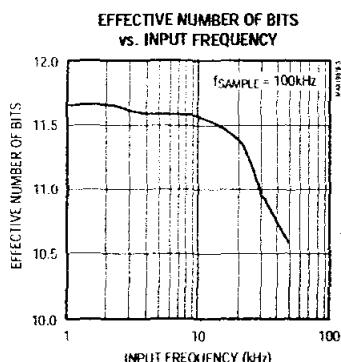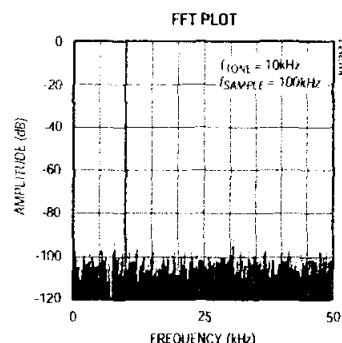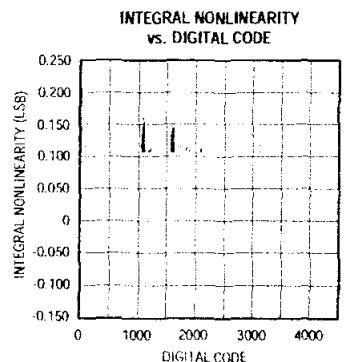
Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS-compatible clock. In internal clock mode, place a capacitor (C_{CLK}) from this pin to ground to set the internal clock frequency: $f_{CLK} = 1.56MHz$ typical with $C_{CLK} = 100pF$.
2	$\overline{CS}$	Chip Select, active low
3-14	D11–D0	Three-State Digital I/O, D11 = MSB
15	AGND	Analog Ground
16-21	CH0-CH5	Analog Input Channels
22	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01μF capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
23	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	$\overline{RD}$	If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
26	$\overline{WR}$	In the internal acquisition mode, when $\overline{CS}$ is low, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. In the external acquisition mode, when $\overline{CS}$ is low, the first rising edge on $\overline{WR}$ starts an acquisition, and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
27	V_{DD}	+5V Supply. Bypass with 0.1μF capacitor to AGND.
28	DGND	Digital Ground

Figure 1. Reference-Adjust Circuit
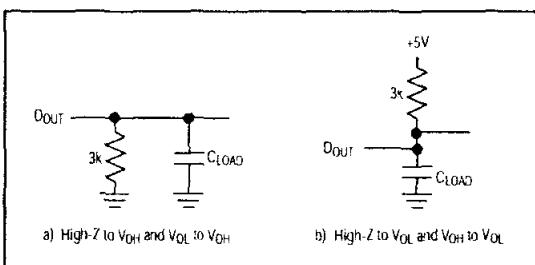
Figure 2. Load Circuits for Enable Time

Detailed Description

Converter Operation

The MAX196/MAX198 multirange, fault-tolerant ADCs use successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The 12-bit parallel-output format provides easy interface to microprocessors (μPs). Figure 3 shows the MAX196/MAX198 in the simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on $\overline{WR}$'s rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. In bipolar mode and unipolar mode (MAX196 only), a low-impedance input source, which settles in less than 1.5μs, is required to maintain conversion accuracy at the maximum conversion rate.

When the MAX198 is configured for unipolar mode, the input does not need to be driven from a low-impedance source. The acquisition time (t_{AZ}) is a function of the source output resistance (R_S), the channel input resistance (R_{IN}), and the T/H capacitance.

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Acquisition time is calculated as follows:

For 0V to V_{REF}: $t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF$

For 0V to $V_{REF}/2$: $t_{AZ} = 9 \times (R_S + R_{IN}) \times 32pF$

where $R_{IN} = 7k\Omega$ and t_{AZ} is never less than 2μs (0V to V_{REF} range) or 3μs (0V to $V_{REF}/2$ range).

In the external acquisition control mode (D5 = 1), the T/H enters its tracking mode on the first $\overline{WR}$ rising edge and enters its hold mode when it detects the second $\overline{WR}$ rising edge with D5 = 0 (see *External Acquisition* section).
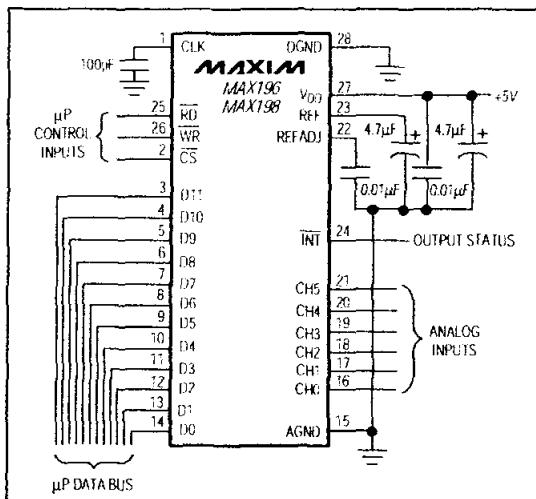
Figure 3. Operational Diagram

S1 = BIPOLAR/UNIPOLAR SWITCH R1 = 12.5kΩ (MAX196) OR 5.12kΩ (MAX198)
S2 = INPUT MUX SWITCH   R2 = 8.67kΩ (MAX196) OR ∞ (MAX198)
S3, S4 = T/H SWITCH
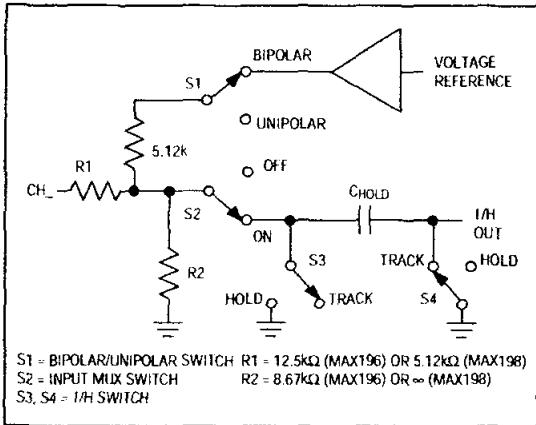
Figure 4. Equivalent Input Circuit

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. The full-scale input voltage depends on the voltage at the reference (V_{REF}). The MAX196 uses a scaling factor, which allows input voltage ranges of ±10V, ±5V, 0V to +10V, or 0V to +5V with a 4.096V voltage reference (Table 1). Program the desired range by setting the appropriate control bits (D3, D4) in the control byte (Tables 2 and 3). The MAX198 does not use a scaling factor, so its input voltage range directly corresponds with the reference voltage. It can be programmed for input voltages of ±V_{REF}, ±$V_{REF}/2$, 0V to V_{REF}, or 0V to $V_{REF}/2$ (Table 3). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ (2.4V < V_{REF} < 4.18V).

The input channels are overvoltage protected to ±16.5V. This protection is active even if the device is in power-down mode.

Even with $V_{DD} = 0V$, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a μP. $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a μP to address the MAX196/MAX198 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Table 1. Full Scale and Zero Scale (MAX196 only)

RANGE (V)	ZERO SCALE (V)	-FULL SCALE	+FULL SCALE
0 to +5	0	—	$V_{REF} \times 1.2207$
0 to +10	0	—	$V_{REF} \times 2.4414$
±5	—	$-V_{REF} \times 1.2207$	$V_{REF} \times 1.2207$
±10	—	$-V_{REF} \times 2.4414$	$V_{REF} \times 2.4414$

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Table 2. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 4).
5	ACQMOD	0 · internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 3).
3	BIP	Selects unipolar or bipolar conversion mode (Table 3).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 5).

Table 3. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V) (MAX196)	INPUT RANGE (V) (MAX198)
0	0	0 to 5	0 to $V_{REF}/2$
0	1	0 to 10	0 to V_{REF}
1	0	±5	$\pm V_{REF}/2$
1	1	±10	$\pm V_{REF}$

Table 4. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD): clock mode is unaffected
1	1	Full Power-Down (FULLPD): clock mode is unaffected

Table 5. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5
0	0	0	*					
0	0	1		*				
0	1	0			*			
0	1	1				*		
1	0	0					*	
1	0	1						*

Multirange, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 2 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading the output data, CS and RD must be low.

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX196/MAX198 for either a unipolar or bipolar input range. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during a conversion cycle will abort the conversion and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3μs with f_{CLK} = 2MHz) ends (see Figure 5).

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode* section).

How to Read a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the device to flag the μP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.
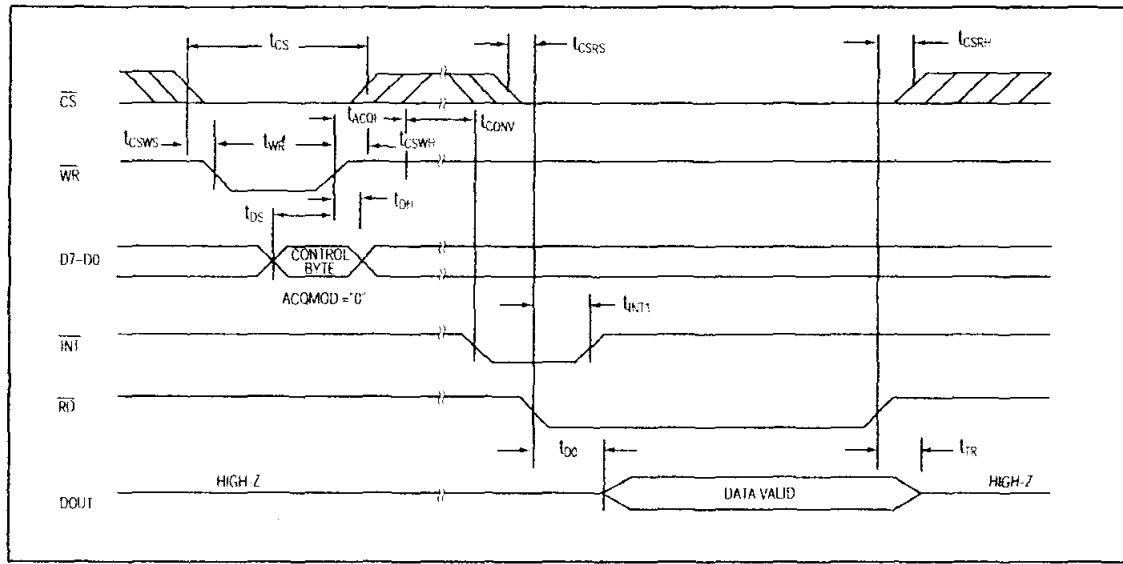

*Figure 5. Conversion Timing Using Internal Acquisition Mode*

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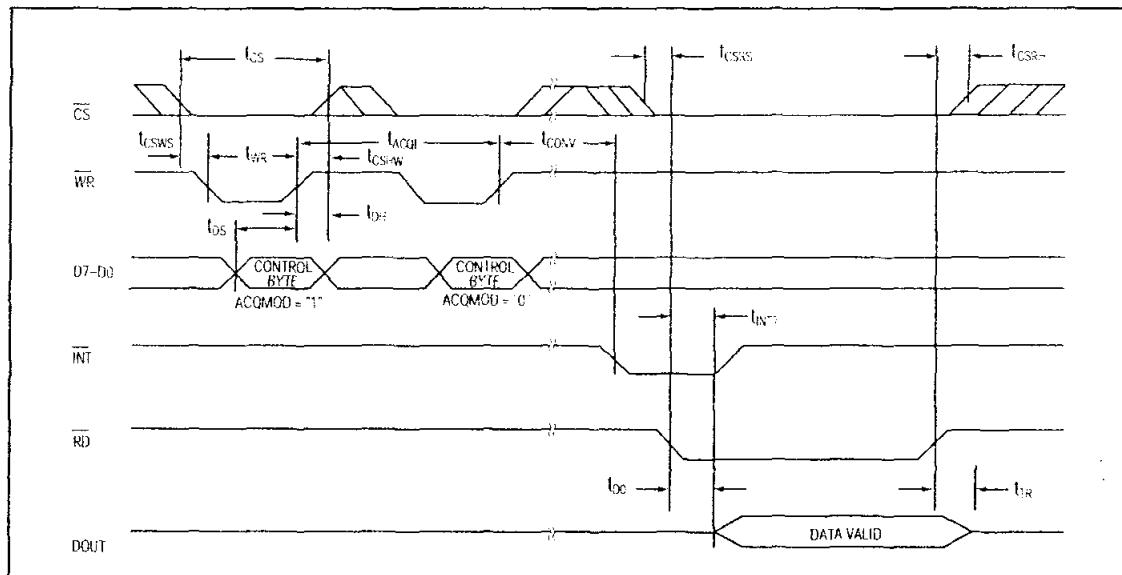
Figure 6. Conversion Timing Using External Acquisition Mode

Clock Modes

The MAX196/MAX198 operate with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, external clock mode is selected.

Internal Clock Mode

Select internal clock mode to free the μP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7 shows a linear relationship between the internal clock period and the value of the external capacitor used.

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and WR timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.
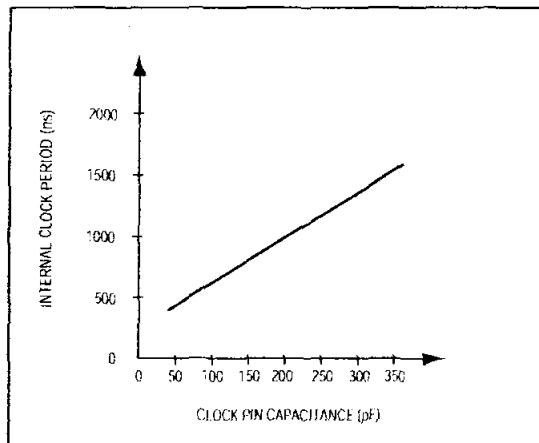
Figure 7. Internal Clock Period vs. Clock Pin Capacitance
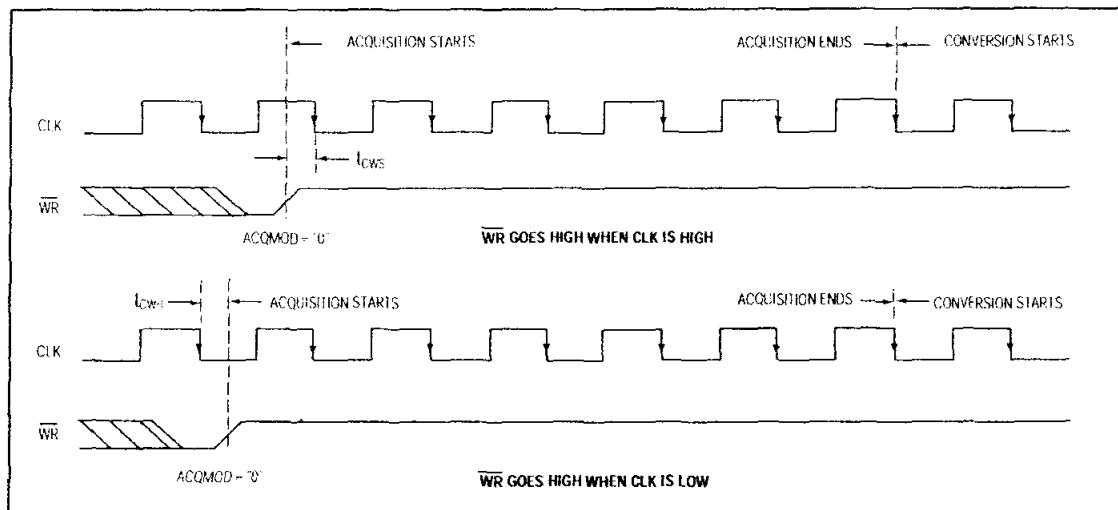
Figure 8a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)
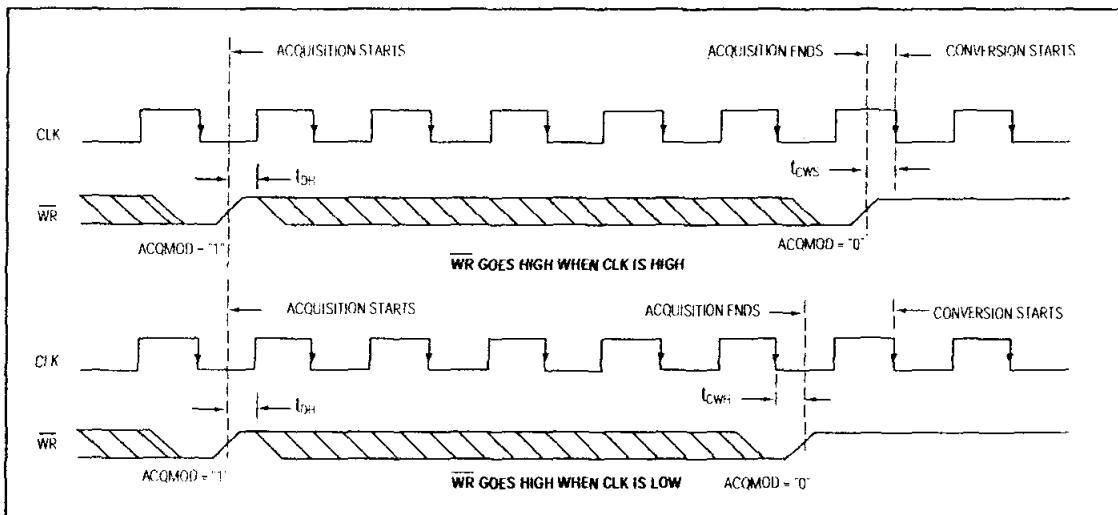
Figure 8b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)

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Applications Information

Power-On Reset

At power-up, the internal power-on reset circuitry sets INT high and puts the device in normal operation/external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX196/MAX198 can operate with either an internal or external reference. An external reference can be connected to either the REF pin or the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to VDD. Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a 4.7µF capacitor to AGND and the REFADJ pin with a 0.01µF capacitor to AGND. The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to deliver 400µA DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value (FS / 4096) results in performance degradation (loss of effective bits).

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available: STBYPD and FULLPD. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion
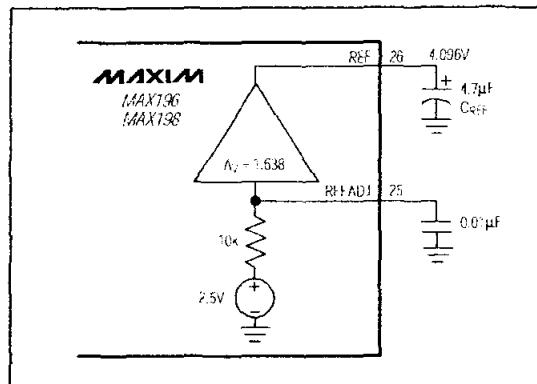

Figure 9a. Internal Reference
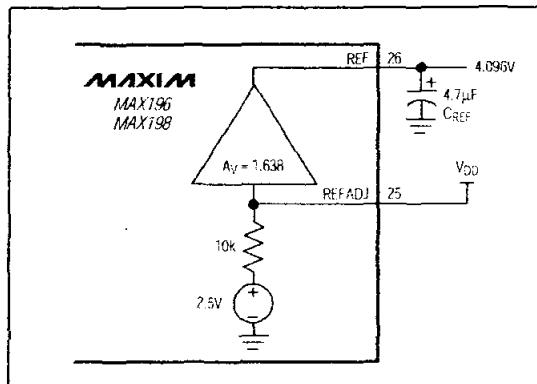

Figure 9b. External Reference, Reference at REF
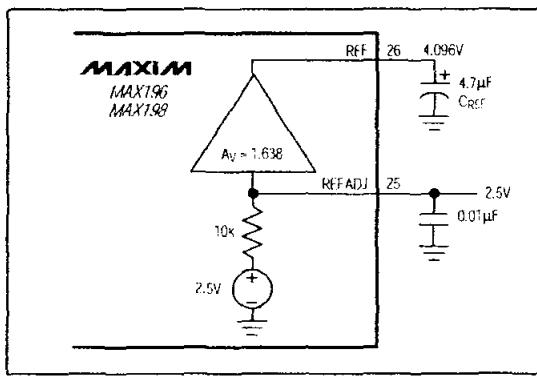
Figure 9c. The external reference overdrives the internal reference.

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results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first WR falling edge during write operation.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversions and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less

than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate, and add 50µs for settling time. Throughput rates of 10ksps offer typical supply currents of 470µA, using the recommended 33µF capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX196/MAX198 down after each conversion without requiring any start-up time on the next conversion.

Transfer Function

Output data coding for the MAX196/MAX198 is binary in unipolar mode with $1LSB = (FS / 4096)$ and twos-complement binary in bipolar mode with $1LSB = [(2 \times |FS|) / 4096]$. Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, refer to Table 1.
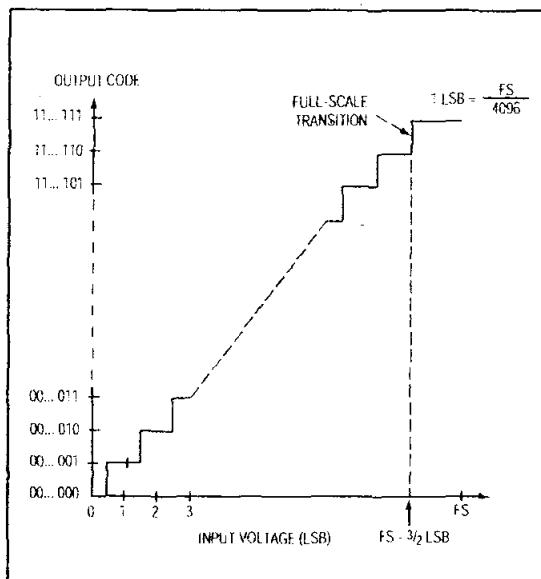
Figure 10. Unipolar Transfer Function
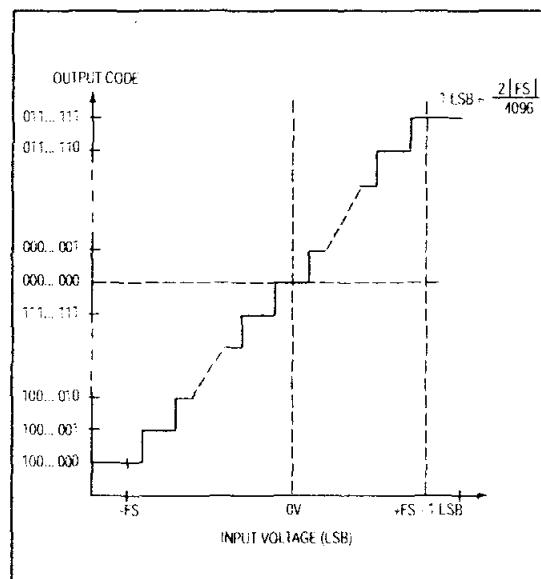
Figure 11. Bipolar Transfer Function

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Layout, Grounding, and Bypassing

Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass VDD with 0.1μF and 4.7μF capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and VDD, as shown in Figure 12.


* OPTIONAL
** CONNECT AGND AND DGND WITH A GROUND PLANE OR A SHORT TRACE
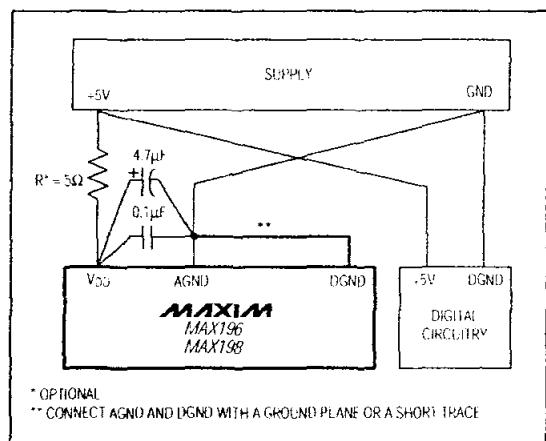
Figure 12. Power-Supply Grounding Connection

Functional Diagram
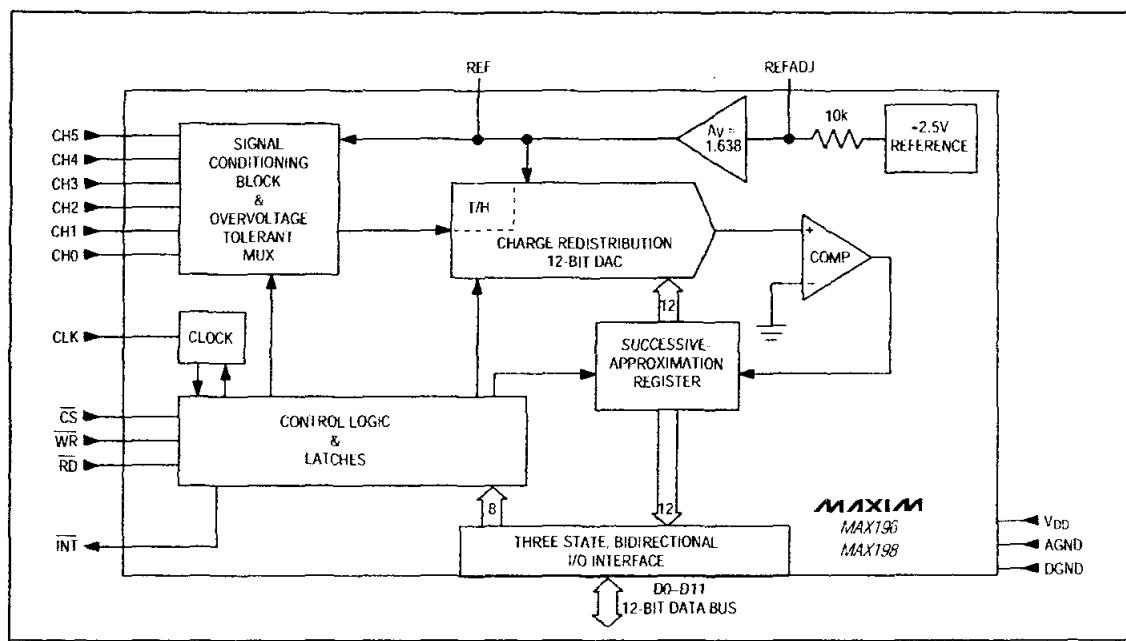
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX196BC/D	0°C to +70°C	Dice*
MAX196AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX196BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX196AEWI	-40°C to +85°C	28 Wide SO
MAX196BEWI	-40°C to +85°C	28 Wide SO
MAX196AEAI	-40°C to +85°C	28 SSOP
MAX196BEAI	-40°C to +85°C	28 SSOP
MAX196AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX196BMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX198ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX198BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX198ACWI	0°C to +70°C	28 Wide SO
MAX198BCWI	0°C to +70°C	28 Wide SO
MAX198ACAI	0°C to +70°C	28 SSOP
MAX198BCAI	0°C to +70°C	28 SSOP
MAX198BC/D	0°C to +70°C	Dice*
MAX198AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX198BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX198AEWI	-40°C to +85°C	28 Wide SO
MAX198BEWI	-40°C to +85°C	28 Wide SO
MAX198AEAI	-40°C to +85°C	28 SSOP
MAX198BEAI	-40°C to +85°C	28 SSOP
MAX198AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX198BMYI	-55°C to +125°C	28 Narrow Ceramic SB**

* Dice are specified at $T_A = +25°C$, DC parameters only.
** Contact factory for availability and processing to MIL-STD-883.

_Chip Topography
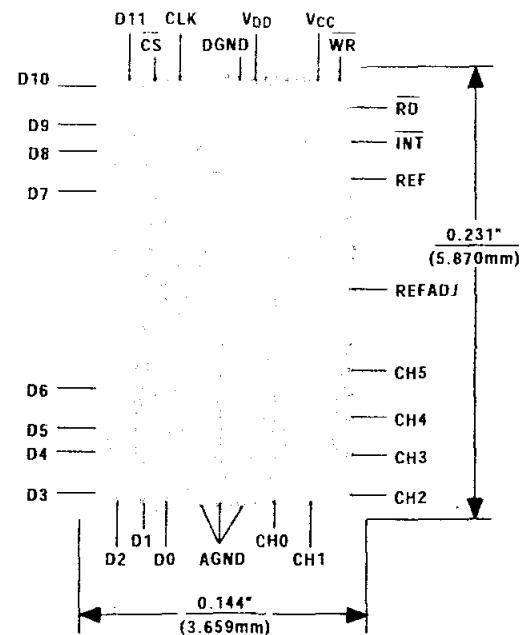
TRANSISTOR COUNT: 2956
SUBSTRATE CONNECTED TO GND

BIODATA

Nama : Budi

NRP : 5103094043

NIRM : 94.7.003.31073.06046

Tempat, Tanggal Lahir : Surabaya, 1 April 1976

Agama : Budha

Alamat : Gembong Sawah III/3, Surabaya

Riwayat Pendidikan :

- Tahun 1988 Lulus SD Kristen Petra II Surabaya.

- Tahun 1991 Lulus SMP Kristen Petra II Surabaya.

- Tahun 1994 Lulus SMA Kristen Petra III Surabaya.

- Tahun 2000 Lulus Sarjana Fakultas Teknik Jurusan Teknik Elektro Universitas Katolik Widya Mandala Surabaya.