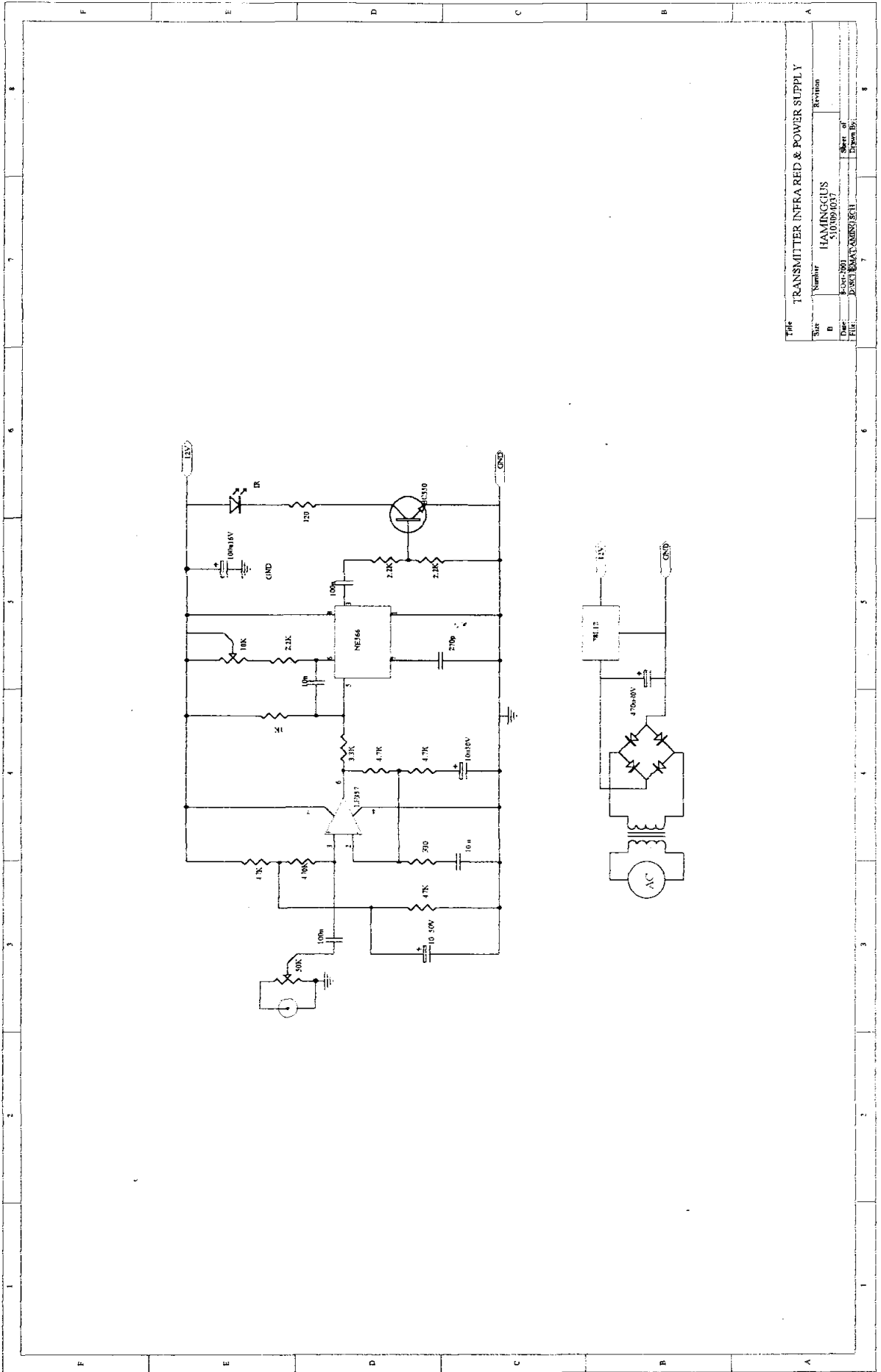
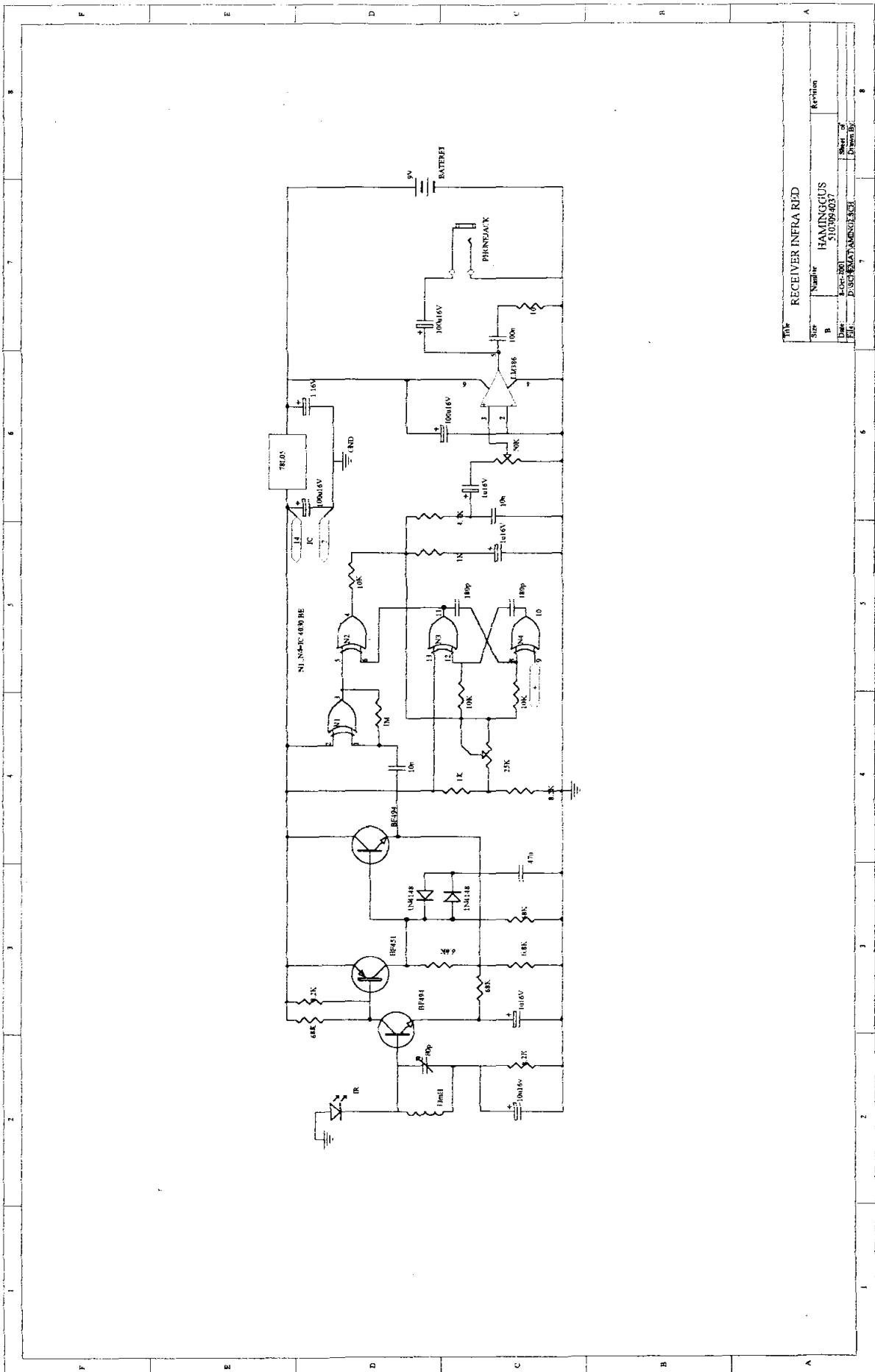


LAMPIRAN A



Title		TRANSMITTER INFRA RED & POWER SUPPLY	
Scale	Number	Author	Revision
B		HAMINGGUS	
Proj.		510.09.0077	
File		2003.05.01.0001.0001	Sheet No.
			Sheet No.



RECEIVER INFRA RED

Site	Number	Revision
B	HAMINGGLUS	
Doc	510099-007	
Proj	D. S. COMPUTER ENGINEERING	Sheet of
		10/20/07

LAMPIRAN B



Industrial/Automotive/Functional Blocks

LM566/LM566C voltage controlled oscillator

general description

The LM566/LM566C are general purpose voltage controlled oscillators which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566 is specified for operation over the -55°C to +125°C military temperature range. The LM566C is specified for operation over the 0°C to +70°C temperature range.

features

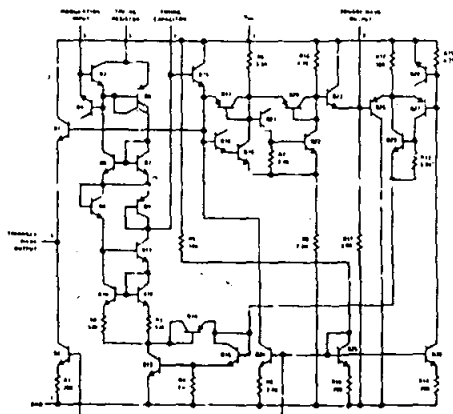
- Wide supply voltage range: 10 to 24 volts
- Very linear modulation characteristics

- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor.

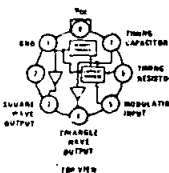
applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

schematic and connection diagrams

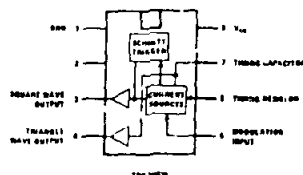


Metal Can Package



Order Number LM566H or LM566CH
See Package 11

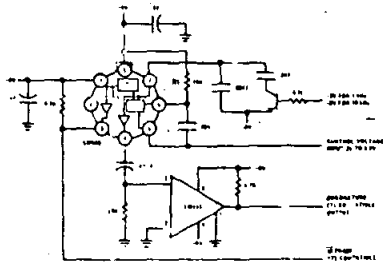
Dual-In-Line Package



Order Number LM566CN
See Package 20

typical application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



applications information

The LM566 may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 4) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A .001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during V_{CO} switching.

$$f_o = \frac{2(V^+ - V_s)}{R_1 C_1 V^+}$$

where

$$2R < R_1 < 20R$$

and V_s is voltage between pin 5 and pin 1

applications information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o = \frac{1}{3.7 R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient".

Loop gain = $K_o K_D \left(\frac{1}{\text{sec}} \right)$

K_c = oscillator sensitivity $\left(\frac{\text{radians/sec}}{\text{volt}} \right)$

K_D = phase detector sensitivity $\left(\frac{\text{volts}}{\text{radian}} \right)$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6 f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit.

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

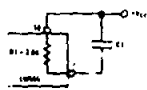
$$f_{H} = \pm \frac{8 f_o}{V_c}$$

f_o = free running frequency of VCO

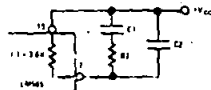
V_c = total supply voltage to the circuit.

THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7) this filter may take one of two forms:



Simple Lag Filter



Lag-Lead Filter

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2} \sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1 C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

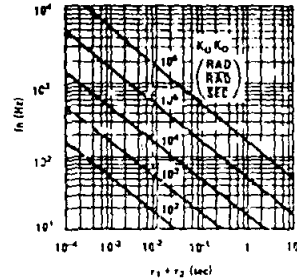
$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

$$\tau_1 + \tau_2 = (R_1 + R_2) C_1$$

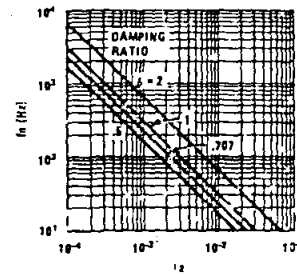
R_2 is selected to produce a desired damping factor δ , usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta = \pi \tau_2 f_n$$

These two equations are plotted for convenience.



Filter Time Constant vs Natural Frequency

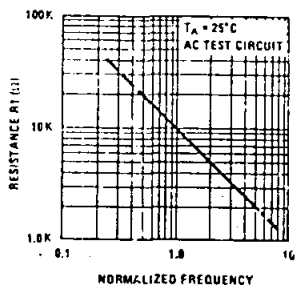


Damping Time Constant vs Natural Frequency

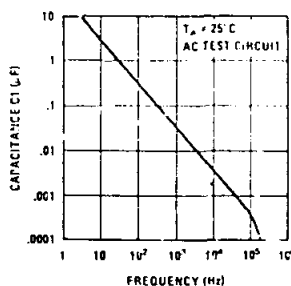
Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1 C_1$.

typical performance characteristics

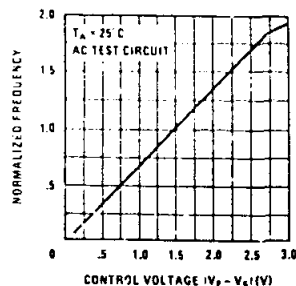
Operating Frequency as a Function of Timing Resistor



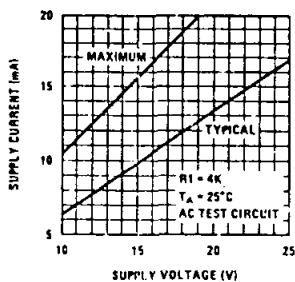
Operating Frequency as a Function of Timing Capacitor



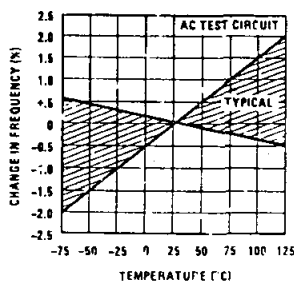
Normalized Frequency as a Function of Control Voltage



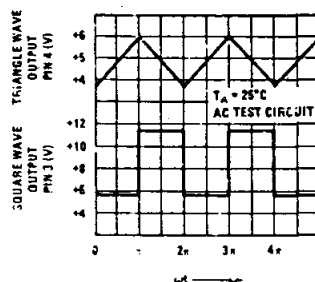
Power Supply Current



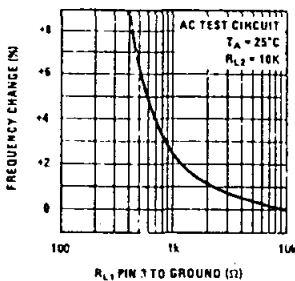
Temperature Stability



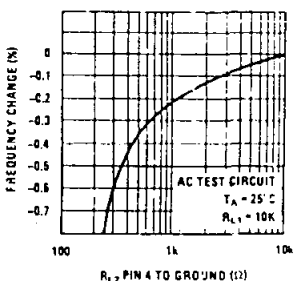
VCO Waveforms



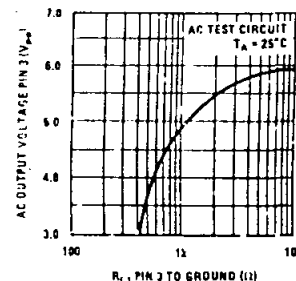
Frequency Stability vs Load Resistance (Square Wave Output)



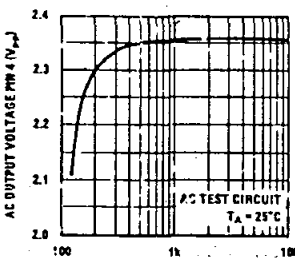
Frequency Stability vs Load Impedance (Triangle Output)



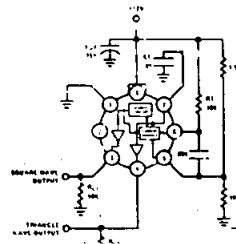
Square Wave Output Characteristics



Triangle Wave Output Characteristics



ac test circuit



absolute maximum ratings

Power Supply Voltage		26V
Power Dissipation (Note 1)		300 mW
Operating Temperature Range	LM566	-55°C to +125°C
	LM566C	0°C to 70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics $V_{CC} = 12V$, $T_A = 25^\circ C$, AC Test Circuit

PARAMETER	CONDITIONS	LM566			LM566C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Operating Frequency	$R_0 = 2k$ $C_0 = 2.7 \mu F$		1			1		MHz
Input Voltage Range Pin 5		$3/4 V_{CC}$		V_{CC}	$3/4 V_{CC}$		V_{CC}	
Average Temperature Coefficient of Operating Frequency			100			200		ppm/°C
Supply Voltage Rejection	10-20V		0.1	1		0.1	2	%/V
Input Impedance Pin 5		0.5	1		0.5	1		MΩ
VCO Sensitivity	For Pin 5, From 8-10V, $f_0 = 10$ kHz	6.4	6.6	6.8	6.0	6.6	7.2	kHz/V
FM Distortion	±10% Deviation		0.2	0.75		0.2	1.5	%
Maximum Sweep Rate		800	1		500	1		MHz
Sweep Range			10:1			10:1		
Output Impedance								
Pin 3			50			50		Ω
Pin 4			50			50		Ω
Square Wave Output Level	$R_L = 10k$	5.0	5.4		5.0	5.4		Vp-p
Triangle Wave Output Level	$R_L = 10k$	2.0	2.4		2.0	2.4		Vp-p
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Triangle Wave Linearity	+1V Segment at $1/2 V_{CC}$		0.2	0.75		0.5	1	%

Note 1: The maximum junction temperature of the LM566 is 150°C, while that of the LM566C is 100°C. For operating at elevated junction temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W. The thermal resistance of the dual-in-line package is 100°C/W.

absolute maximum ratings

Input Voltage: $V_O = 5V$ to $8V$	30V	Maximum Junction Temperature	150°C
$V_O = 12V$ to $18V$	35V	Storage Temperature Range	
$V_O = 24V$	40V	Metal Can (H Package)	-65°C to +150°C
Internal Power Dissipation (Note 1)	Internally Limited	Molded TO-92	-55°C to +150°C
Operating Temperature Range	0°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2) $T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$, $I_O = 40\text{ mA}$, $C_{IN} = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ (unless noted)

LM78LXXAC OUTPUT VOLTAGE		5V			6V			8V			10V			12V			15V			18V			24V			UNITS												
INPUT VOLTAGE (unless other wise noted)		10V			11V			14V			17V			19V			23V			27V			33V															
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX													
V_O Output Voltage (Note 4)	$T_J = 25^\circ\text{C}$	4.8	5	5.2	6.75	6	6.75	7.7	8	8.3	9.6	10	10.4	11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23	24	25	V												
	$1\text{ mA} \leq I_O \leq 70\text{ mA}$	4.75	5.25		6.7	6.3		7.6	8.4		9.5	10.5		11.4	12.6		14.25	15.75		17.2	18.9		22.8	25.2		V												
	$1\text{ mA} \leq I_O \leq 40\text{ mA}$ and $V_{MIN} \leq V_{IN} \leq V_{MAX}$	4.75	5.25		6.7	6.2		7.6	8.4		9.5	10.5		11.4	12.6		14.25	15.75		17.2	18.9		22.8	25.2		V												
ΔV_O Line Regulation	$T_J = 25^\circ\text{C}$	$(7 \leq V_{IN} \leq 20)$			$(8.3 \leq V_{IN} \leq 21)$			$(10.5 \leq V_{IN} \leq 23)$			$(12.5 \leq V_{IN} \leq 25)$			$(14.5 \leq V_{IN} \leq 27)$			$(17.5 \leq V_{IN} \leq 30)$			$(20.7 \leq V_{IN} \leq 33)$			$(27 \leq V_{IN} \leq 38)$		mV													
		$(8 \leq V_{IN} \leq 20)$		10	54		$(8 \leq V_{IN} \leq 21)$		10	68		$(11 \leq V_{IN} \leq 23)$		12	85		$(13 \leq V_{IN} \leq 25)$		16	105		$(16 \leq V_{IN} \leq 27)$		20	110		25	140		35	190		50	200				
		$(7 \leq V_{IN} \leq 20)$		18	75		$(8.3 \leq V_{IN} \leq 21)$		18	96		$(10.5 \leq V_{IN} \leq 23)$		20	100		$(12.5 \leq V_{IN} \leq 25)$		25	140		$(14.5 \leq V_{IN} \leq 27)$		30	180		$(17.5 \leq V_{IN} \leq 30)$		37	250		45	275		60	300		
ΔV_O Load Regulation	$T_J = 25^\circ\text{C}$, $1\text{ mA} \leq I_O \leq 40\text{ mA}$	$(7 \leq V_{IN} \leq 20)$		5	30		$(8 \leq V_{IN} \leq 21)$		6	35		$(10.5 \leq V_{IN} \leq 23)$		8	40		$(12.5 \leq V_{IN} \leq 25)$		9	45		$(14.5 \leq V_{IN} \leq 27)$		10	50		12	75		15	85		20	100				
		$(7 \leq V_{IN} \leq 20)$		20	60		$(8.3 \leq V_{IN} \leq 21)$		22	70		$(10.5 \leq V_{IN} \leq 23)$		25	80		$(12.5 \leq V_{IN} \leq 25)$		27	90		$(14.5 \leq V_{IN} \leq 27)$		30	100		35	150		40	170		50	200				
ΔV_O Long Term Stability		12			15			20			22			24			30			45			56			mV/1000 hrs												
I_O Quiescent Current	$T_J = 25^\circ\text{C}$	$(7 \leq V_{IN} \leq 20)$		3	5		$(8.3 \leq V_{IN} \leq 21)$		3	5		$(10.5 \leq V_{IN} \leq 23)$		3	5		$(12.5 \leq V_{IN} \leq 25)$		3	5		$(14.5 \leq V_{IN} \leq 27)$		3	5		3	5		3	5		3	5				
		$(7 \leq V_{IN} \leq 20)$			4.7		$(8.3 \leq V_{IN} \leq 21)$			4.7		$(10.5 \leq V_{IN} \leq 23)$			4.7		$(12.5 \leq V_{IN} \leq 25)$			4.7		$(14.5 \leq V_{IN} \leq 27)$			4.7			4.7			4.7			4.7				
ΔI_O Quiescent Current Change	$1\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_{MIN} \leq V_{IN} \leq V_{MAX}$	0.1			0.1			0.1			0.1			0.1			0.1			0.1			0.1			mA												
		$(8 \leq V_{IN} \leq 20)$		1.0	$(8 \leq V_{IN} \leq 21)$		1.0	$(11 \leq V_{IN} \leq 23)$		1.0	$(13 \leq V_{IN} \leq 25)$		1.0	$(16 \leq V_{IN} \leq 27)$		1.0	$(20 \leq V_{IN} \leq 30)$		1.0	$(27 \leq V_{IN} \leq 33)$		1.0	$(27 \leq V_{IN} \leq 38)$		1.0	$(27 \leq V_{IN} \leq 38)$		1.0	$(27 \leq V_{IN} \leq 38)$		1.0	$(27 \leq V_{IN} \leq 38)$		1.0				
V_n Output Noise Voltage	$T_J = 25^\circ\text{C}$, (Note 3) $f = 10\text{ Hz} - 10\text{ kHz}$	40			50			60			70			80			90			150			200			μV												
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ Ripple Rejection	$f = 120\text{ Hz}$	$(8 \leq V_{IN} \leq 16)$		47	62		$(8 \leq V_{IN} \leq 18)$		45	60		$(12 \leq V_{IN} \leq 23)$		43	57		$(13 \leq V_{IN} \leq 25)$		41	55		$(15 \leq V_{IN} \leq 25)$		40	54		$(18.5 \leq V_{IN} \leq 28.5)$		37	51		$(23 \leq V_{IN} \leq 33)$		36	48		34	45
		$(8 \leq V_{IN} \leq 16)$					$(8 \leq V_{IN} \leq 18)$					$(12 \leq V_{IN} \leq 23)$					$(13 \leq V_{IN} \leq 25)$					$(15 \leq V_{IN} \leq 25)$					$(18.5 \leq V_{IN} \leq 28.5)$					$(23 \leq V_{IN} \leq 33)$						
Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ\text{C}$	7			8.3			10.5			12.5			14.5			17.5			20.7			27			V												

Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is 40°C/W junction to case and 140°C/W junction to ambient. Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3: Recommended minimum load capacitance of 0.01 μF to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within $\pm 0.01\% V_O/^\circ\text{C}$.



Voltage Regulators

LM78LXX series three terminal positive regulators

general description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78LXX is available in the metal three lead TO-5 (H) and the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes

too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

features

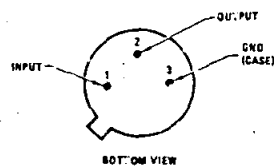
- Output voltage tolerances of $\pm 5\%$ (LM78LXXAC) and $\pm 10\%$ (LM78LXXC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 low profile packages

voltage range

LM78L05	5V	LM78L12	12V
LM78L06	6V	LM78L15	15V
LM78L08	8V	LM78L18	18V
LM78L10	10V	LM78L24	24V

connection diagrams

Metal Can Package

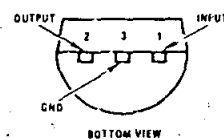


Order Numbers:

LM78L05ACH	LM78L05CH
LM78L06ACH	LM78L06CH
LM78L08ACH	LM78L08CH
LM78L10ACH	LM78L10CH
LM78L12ACH	LM78L12CH
LM78L15ACH	LM78L15CH
LM78L18ACH	LM78L18CH
LM78L24ACH	LM78L24CH

See Package 9

Plastic Package

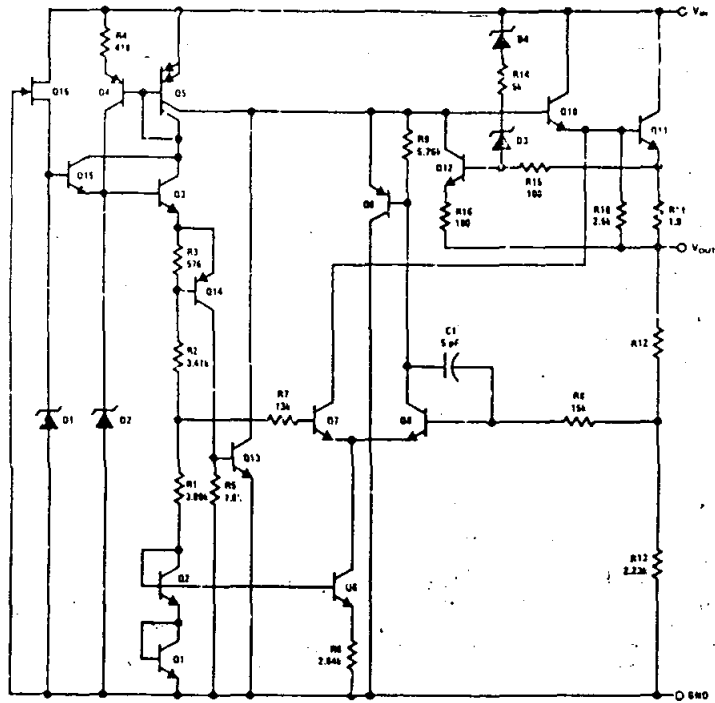


Order Numbers:

LM78L05ACZ	LM78L05CZ
LM78L06ACZ	LM78L06CZ
LM78L08ACZ	LM78L08CZ
LM78L10ACZ	LM78L10CZ
LM78L12ACZ	LM78L12CZ
LM78L15ACZ	LM78L15CZ
LM78L18ACZ	LM78L18CZ
LM78L24ACZ	LM78L24CZ

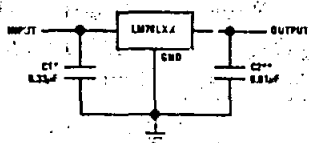
See Package 38

Equivalent Circuit



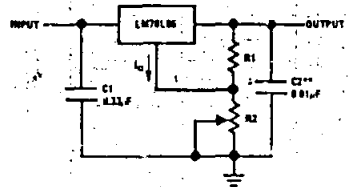
LM78LXX

typical applications



*Required if the regulator is located far from the power supply filter.
 **See Table 3 in the electrical characteristics table.

Fixed Output Regulator

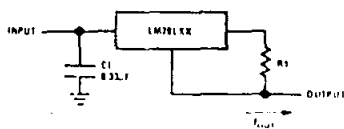


$$V_{out} = 6V + (V_{in} - 1)V_{ADJ}$$

$$V_{in} > 2V_{out} \text{ (load regulation (L))} = (R1 + R2/R1) I_L \text{ of LM78L06}$$

Adjustable Output Regulator

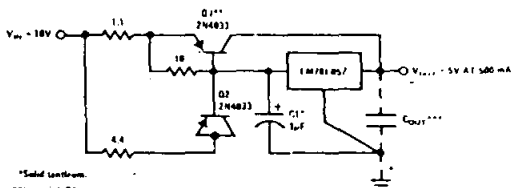
typical applications (con't)



$$I_{OUT} = (V_{I1}/R_L) + I_Q$$

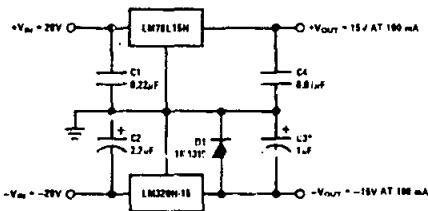
$\Delta I_Q = 1.5 \text{ mA}$ over line and load changes

Current Regulator



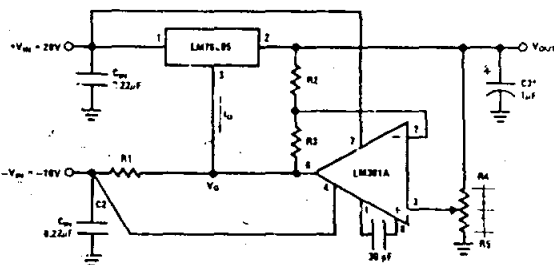
*Solid spectrum.
 **Heat sink 01.
 ***Optional: Improves ripple rejection and transient response.
 Load Regulation: 0.8% $0 \leq I_L \leq 250 \text{ mA}$ period with $I_{OUT} = 50 \text{ mA}$.

5V, 500 mA Regulator with Short Circuit Protection



*Solid spectrum.

±15V, 100 mA Dual Power Supply



*Solid spectrum.
 $V_{OUT} = 5V + 5V \cdot R1 / (R1 + R2 + R3 + R4 + R5)$
 $V_{OUT} = 5V (R1/R4)$ for $(R2 + R3 + R4 + R5) \gg R1$
 A 0.5V output will require $R1 = (R2 + R3 + R4 + R5) \cdot 0.1$

Variable Output Regulator 0.5V - 18V

absolute maximum ratings

Input Voltage	$V_O = 5V$ to $8V$	30V	Maximum Junction Temperature	150°C
	$V_O = 12V$ to $18V$	35V	Storage Temperature Range	
	$V_O = 24V$	40V	Metal Can (H Package)	-65°C to +150°C
Internal Power Dissipation (Note 1)		Internally Limited	Molded TO-92	-55°C to +150°C
Operating Temperature Range		0°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2) $T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$, $I_O = 40\text{ mA}$, $C_{IN} = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ (unless noted)

LM78LXX OUTPUT VOLTAGE		5V	6V	8V	10V	12V	15V	18V	24V	U"II																
INPUT VOLTAGE (unless otherwise noted)		10V	11V	14V	17V	19V	23V	27V	33V																	
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX																
V_O Output Voltage (Note 4)	$T_J = 25^\circ\text{C}$	4.6	5	5.4	5.5	6	6.5	7.36	8	8.64	9.2	10	10.8	11.1	12	12.9	13.8	15	16.2	16.6	18	19.4	22.1	24	25.0	
	$1\text{ mA} \leq I_O \leq 70\text{ mA}$ or $1\text{ mA} \leq I_O \leq 40\text{ mA}$ and ΔV_{IN}	4.5	5.5	5.4	6.6	7.2	8.8	9.0	11	10.8	13.2	13.5	16.5	16.2	19.8	21.4	26.4									
			(7 $\leq V_{IN} \leq 20$)		(8.5 $\leq V_{IN} \leq 21$)		(10.5 $\leq V_{IN} \leq 23$)		(13 $\leq V_{IN} \leq 25$)		(14.5 $\leq V_{IN} \leq 27$)		(18 $\leq V_{IN} \leq 30$)		(21.4 $\leq V_{IN} \leq 33$)		(28 $\leq V_{IN} \leq 38$)									
ΔV_O Line Regulation	$T_J = 25^\circ\text{C}$	10	150	10	150	12	150	16	175	20	200	25	250	27	275	30	300									
		8 $\leq V_{IN} \leq 20$		9 $\leq V_{IN} \leq 21$		11 $\leq V_{IN} \leq 23$		14 $\leq V_{IN} \leq 25$		18 $\leq V_{IN} \leq 27$		20 $\leq V_{IN} \leq 30$		22 $\leq V_{IN} \leq 33$		28 $\leq V_{IN} \leq 38$										
		18	200	18	200	20	200	25	225	30	250	30	300	32	325	35	350									
		(7 $\leq V_{IN} \leq 20$)		(8.5 $\leq V_{IN} \leq 21$)		(10.5 $\leq V_{IN} \leq 23$)		(13 $\leq V_{IN} \leq 25$)		(14.5 $\leq V_{IN} \leq 27$)		(18 $\leq V_{IN} \leq 30$)		(21.4 $\leq V_{IN} \leq 33$)		(27.5 $\leq V_{IN} \leq 38$)										
ΔV_L Load Regulation	$T_J = 25^\circ\text{C}$, $1\text{ mA} \leq I_O \leq 40\text{ mA}$ $T_J = 25^\circ\text{C}$, $1\text{ mA} \leq I_O \leq 100\text{ mA}$	5	30	6	35	8	40	9	45	10	60	12	75	15	85	20	100									
		20	60	22	70	25	80	27	90	30	130	35	150	40	170	40	200									
ΔV_O Long Term Stability		12		15		20		22		24		30		45		56										mV/10%
I_O Quiescent Current	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	3	6	3	6	3	6	3	6	3	6.5	3.1	6.5	3.1	6.5	3.1	6.5									
			5.5		5.5		5.5		5.5		8		6		6		6									
I_{IQ} Quiescent Current	$T_J = 25^\circ\text{C}$, $1\text{ mA} \leq I_O \leq 40\text{ mA}$	0.2		0.2		0.2		0.2		0.2		0.2		0.2		0.2										
			1.5		1.5		1.5		1.5		1.5		1.5		1.5		1.5									
V_{IN} Output Noise Voltage	$T_J = 25^\circ\text{C}$, (Note 3) $f = 10\text{ Hz} - 10\text{ kHz}$	40		50		60		70		80		90		150		200										
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ Ripple Rejection	$f = 125\text{ Hz}$	40	60	38	58	36	55	36	53	35	52	33	49	32	46	30	43									
				(8 $\leq V_{IN} \leq 20$)		(9 $\leq V_{IN} \leq 21$)		(11 $\leq V_{IN} \leq 23$)		(14 $\leq V_{IN} \leq 25$)		(15 $\leq V_{IN} \leq 25$)		(18.5 $\leq V_{IN} \leq 28.5$)		(23 $\leq V_{IN} \leq 33$)		(29 $\leq V_{IN} \leq 35$)								
Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ\text{C}$	7		8.3		10.5		13		14.5		18		21.4		27.5										

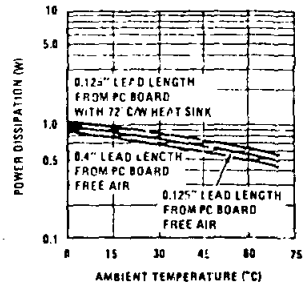
Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is 40°C/W junction to case and 140°C/W junction to ambient. Thermal resistance of the TO-92 package is 180°C/W junction to ambient with $0.4''$ leads from a PC board and 160°C/W junction to ambient with $0.125''$ lead length to a PC board.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

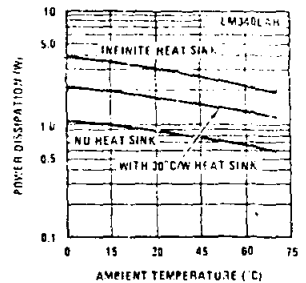
Note 3: Recommended minimum load capacitance of $0.01\mu\text{F}$ to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within $\pm 0.01\%$ $V_O/^\circ\text{C}$.

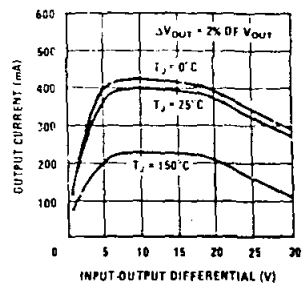
Maximum Average Power Dissipation (Plastic Package)



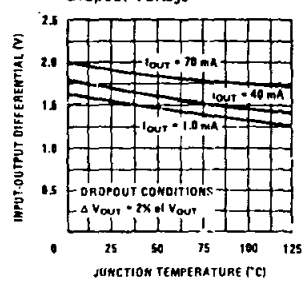
Maximum Average Power Dissipation (Metal Can Package)



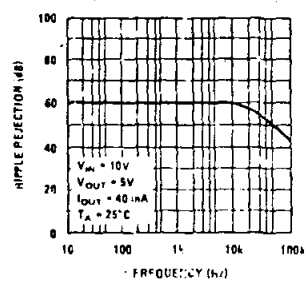
Peak Output Current



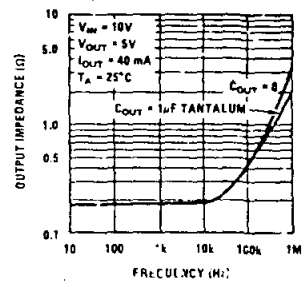
Dropout Voltage



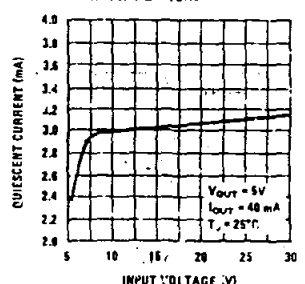
Ripple Rejection



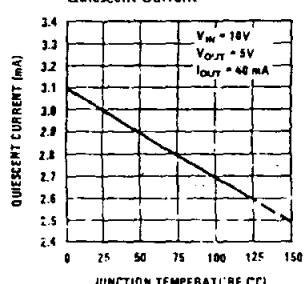
Output Impedance



Quiescent Current



Quiescent Current



LF147/LF347/LF347B

Typical Applr

**Jctor
157 Series Monolithic
ational Amplifiers**

55/LF355/LF355A/
/ Current
56/LF356/LF356A/

LF147/LF347/LF347B

LF155/155A/LF255/LF355/355A/355B/LF156/LF256/LF356/LF356A/356B/LF157

57/LF357/LF357A/

**LF357B Wide Band Decompensated ($A_{V_{MIN}} = 5$)
General Description**

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

- Photocell amplifiers
- Sample and Hold circuits

Common Features

(LF155A, LF156A, LF157A)

- Low input bias current 30 pA
- Low Input Offset Current 3 pA
- High input impedance $10^{12} \Omega$
- Low input offset voltage 1 mV
- Low input offset voltage temp. drift $3 \mu V/^{\circ}C$
- Low input noise current $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- High common-mode rejection ratio 100 dB
- Large dc voltage gain 106 dB

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

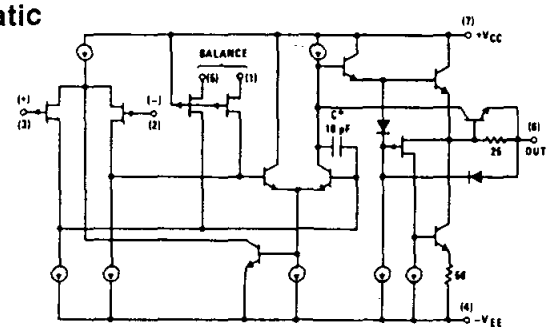
Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	$V/\mu s$
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{\text{Hz}}$

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

Simplified Schematic



*3 pF in LF157 series.

TL/H/5646-1

LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/LF356A/356B/LF157/157A/LF257/LF357/357A/357B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/ LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
J-Package		150°C	115°C	115°C
M-Package			100°C	100°C
Power Dissipation at $T_A = 25^\circ\text{C}$ (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
J-Package		1260 mW	900 mW	900 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
J-Package		100°C/W	100°C/W	100°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance				
(100 pF discharged through 1.5 k Ω)	1200V	1200V	1200V	1200V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25^\circ\text{C}$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	$\mu\text{V}/^\circ\text{C}$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{OS}	Input Offset Current	$T_j = 25^\circ\text{C}$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25^\circ\text{C}$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25^\circ\text{C}$		10 ¹²			10 ¹²		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$ Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

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LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/356A/356B/LF157/157A/LF257/LF357/357A/357B

DC Electrical Characteristics (Note 3) $T_A = T_J = 25^\circ\text{C}$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15\text{V}$	± 11	+15.1 -12		± 11	+15.1 -12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12					V/ μs V/ μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$		25 25			15 12			15 12		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent Input Noise Current	$f = 100\text{ Hz}$ $f = 1000\text{ Hz}$		0.01 0.01			0.01 0.01			0.01 0.01		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu\text{V}/^\circ\text{C}$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{OS}	Input Offset Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_J = 25^\circ\text{C}$, (Notes 3, 5) $T_J \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_J = 25^\circ\text{C}$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$ Over Temperature	50	200		50	200		25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15\text{V}$	± 11	+15.1 -12		± 11	+15.1 -12		+10	+15.1 -12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_J = 25^\circ\text{C}, V_S = \pm 15\text{V}$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157, LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_J = 25^\circ\text{C}, V_S = \pm 15\text{V}$

Symbol	Parameter	Conditions	LF155/255/355/355B	LF156/256, LF356B	LF156/256/356/356B	LF157/257, LF357B	LF157/257/357/357B	Units
			Typ	Min	Typ	Min	Typ	
s_r	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/ μs V/ μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$	25 20		15 12		15 12	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent Input Current Noise	$f = 100\text{ Hz}$ $f = 1000\text{ Hz}$	0.01 0.01		0.01 0.01		0.01 0.01	pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
C_{in}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

- Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the $25^\circ\text{C } P_{D(MAX)}$, whichever is less.
- Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- Note 3: Unless otherwise stated, these test conditions apply:

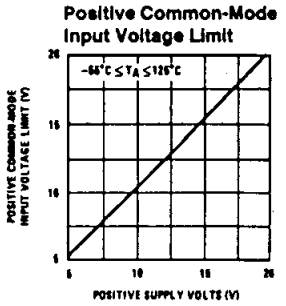
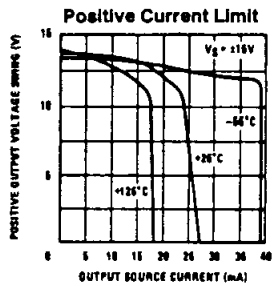
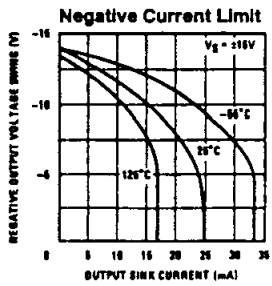
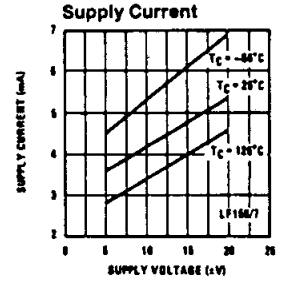
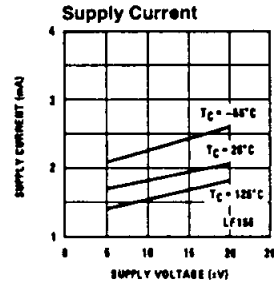
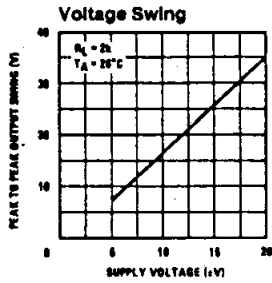
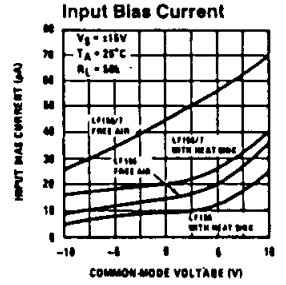
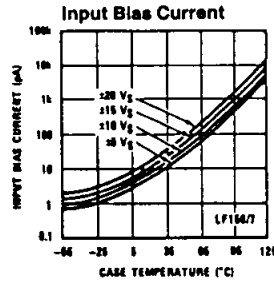
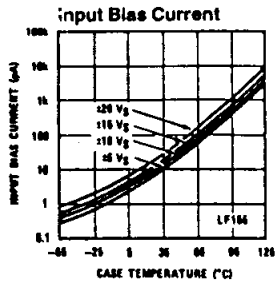
	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 18\text{V}$	$\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$	$V_S = \pm 15\text{V}$
T_A	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

- and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.
- Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
- Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_J = T_A + \theta_{JA} P_d$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
- Note 7: Settling time is defined here, for a unity gain inverter connection using 2 k Ω resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 k Ω and the output step is 10V (See Settling Time Test Circuit).
- Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETSF156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.
- Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

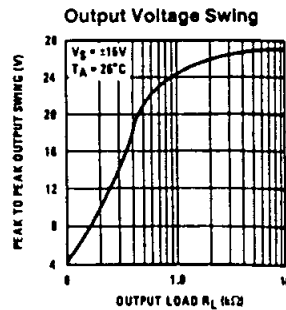
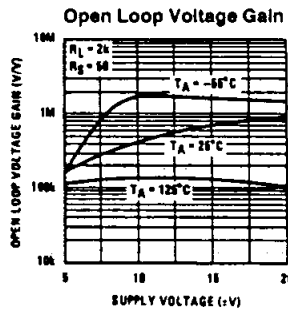
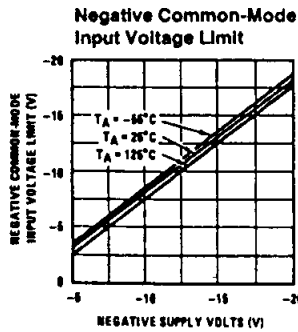
LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/356B/LF157/157A/LF257/LF357/357A/357B

Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

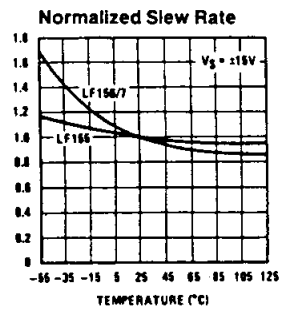
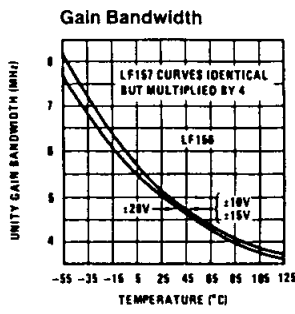
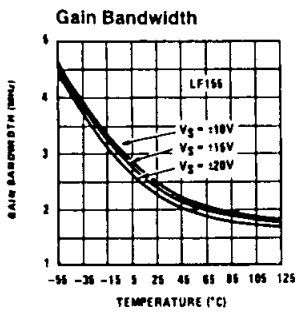


TL/H/5646-1

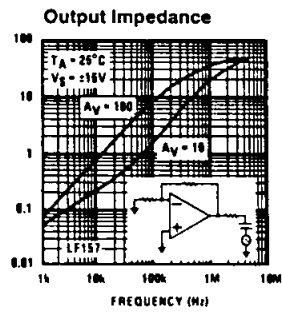
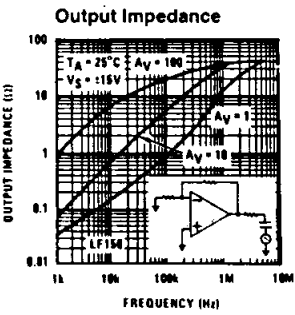
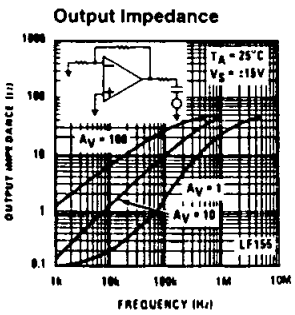


TL/H/5646-1

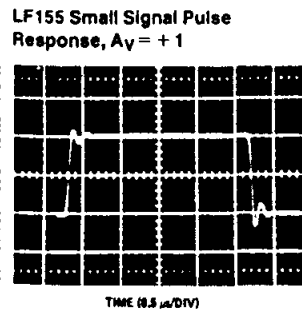
Typical AC Performance Characteristics



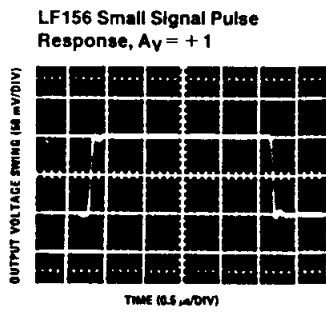
TL/H/5646-4



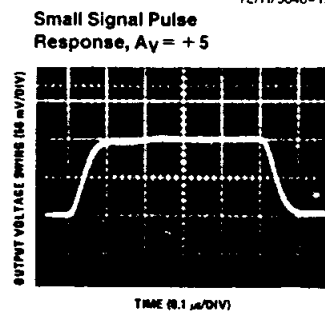
TL/H/5646-12



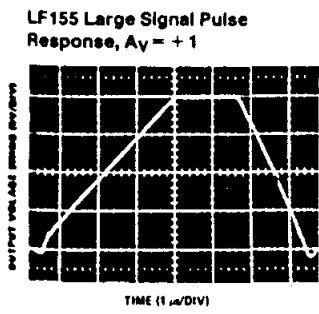
TL/H/5646-5



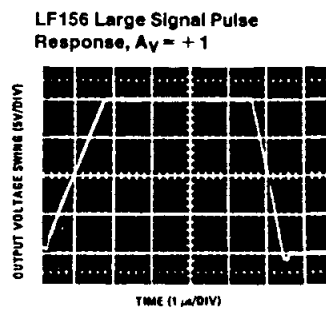
TL/H/5646-6



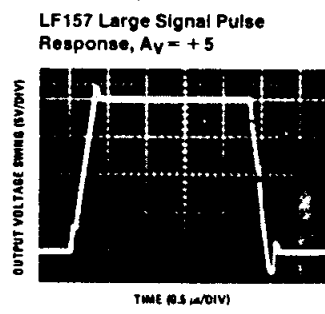
TL/H/5646-7



TL/H/5646-8



TL/H/5646-9

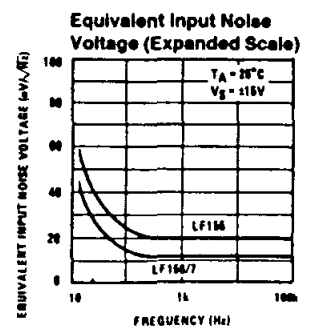
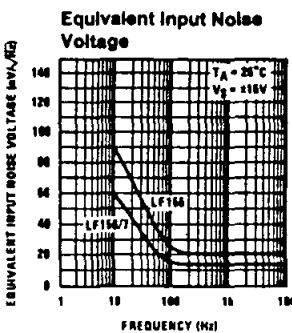
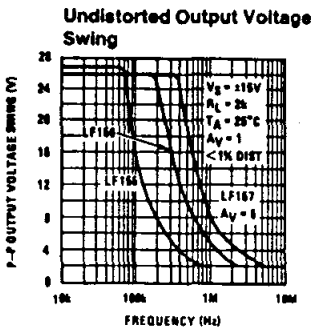
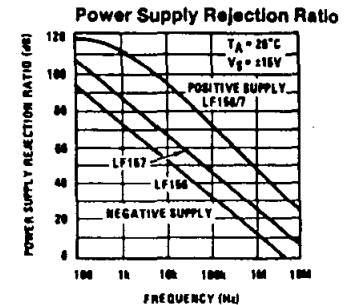
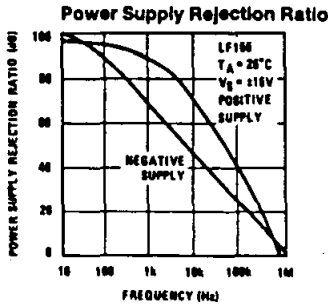
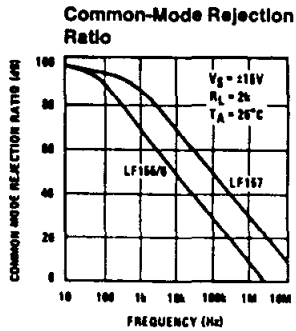
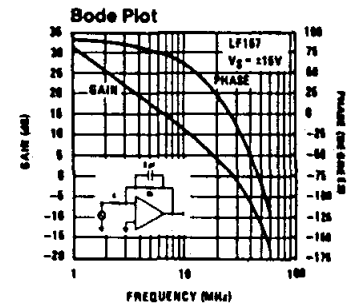
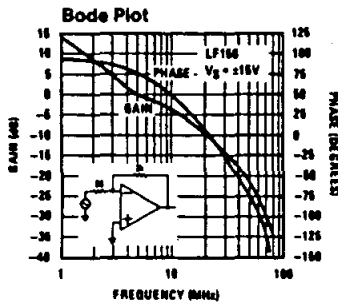
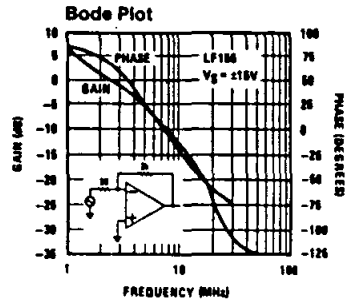
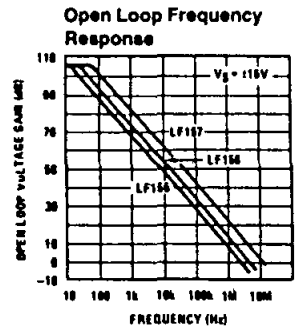
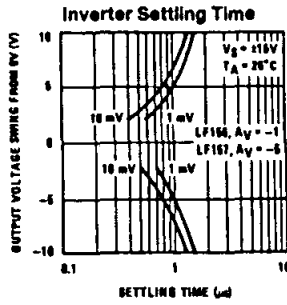
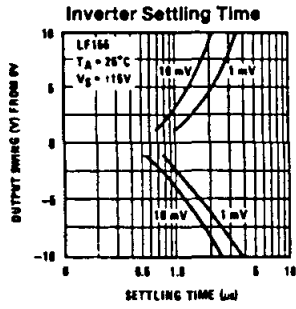


TL/H/5646-10

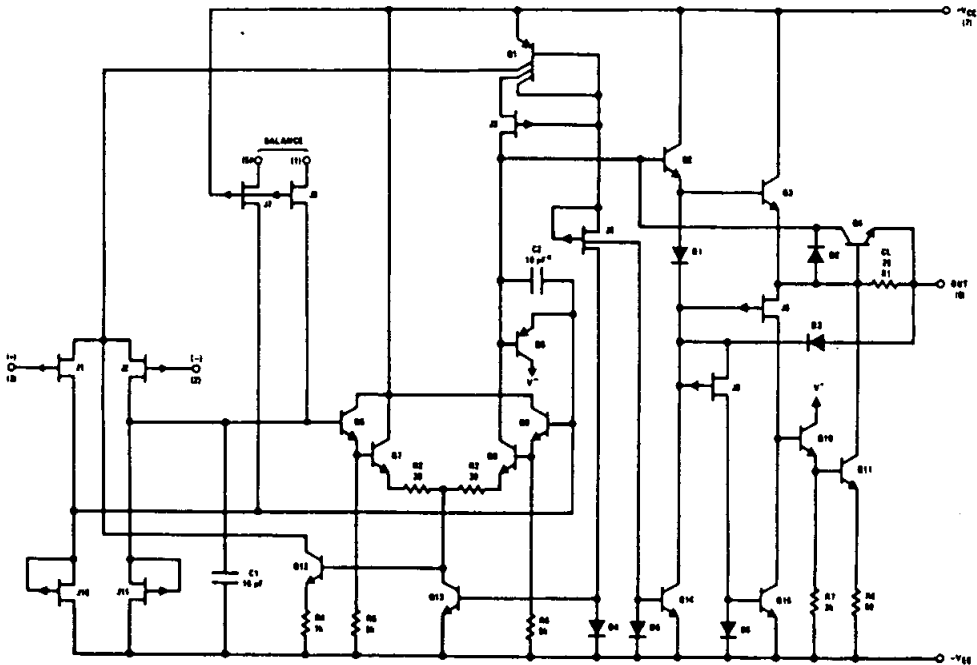
LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/LF356A/356B/LF157/157A/LF257/LF357/357A/357B

LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/356A/356B/LF157/157A/LF257/LF357/357A/357B

Typical AC Performance Characteristics (Continued)



Detailed Schematic

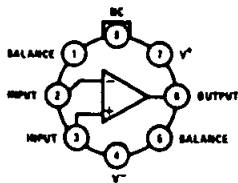


*C = 3 pF in LF157 series.

TL/H/5645-13

Connection Diagrams (Top Views)

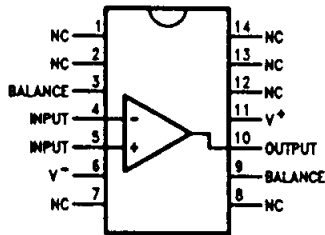
Metal Can Package (H)



TL/H/5646-14

Order Number
 LF155AH, LF156AH, LF157AH,
 LF155H, LF156H, LF157H,
 LF255H, LF256H, LF257H,
 LF355AH, LF356AH, LF357AH,
 LF355BH, LF356BH, LF357BH,
 LF355H, LF356H or LF357H
 See NS Package Number H08C

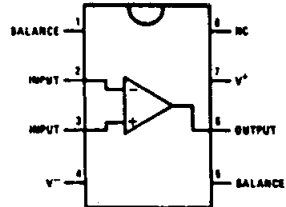
Dual-in-Line Package (J)



TL/H/5646-30

Order Number
 LF155J, LF156J, LF157J,
 LF355J, LF356J, LF357J,
 LF355BJ, LF356BJ or LF357BJ
 See NS Package Number J14A

Dual-in-Line Package (M and N)



TL/H/7 46-29

Order Number
 LF355M, LF356M, LF357M,
 LF356BM, LF355BN, LF356BN,
 LF357BN, LF355N, LF356N or
 LF357N
 See NS Package Number
 M08A or N08E

LF155/155A/LF255/LF355/355A/355B/LF156/156A/LF256/LF356/LF356A/356B/LF157/157A/LF257/LF357/357A/357B



Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in

polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

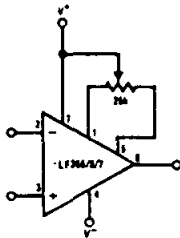
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

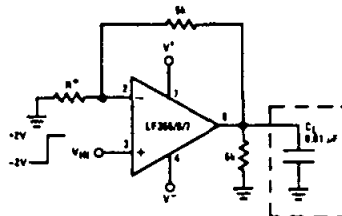
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V⁺
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5 \mu\text{V}/^\circ\text{C}/\text{mV}$ of adjustment
- Typical overall drift: $5 \mu\text{V}/^\circ\text{C} \pm (0.5 \mu\text{V}/^\circ\text{C}/\text{mV}$ of adj.)

Driving Capacitive Loads



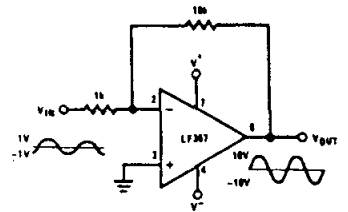
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(\text{MAX})} \approx 0.01 \mu\text{F}$.

Overshoot $\leq 20\%$

Setting time (t_s) $\approx 5 \mu\text{s}$

LF157. A Large Power BW Amplifier

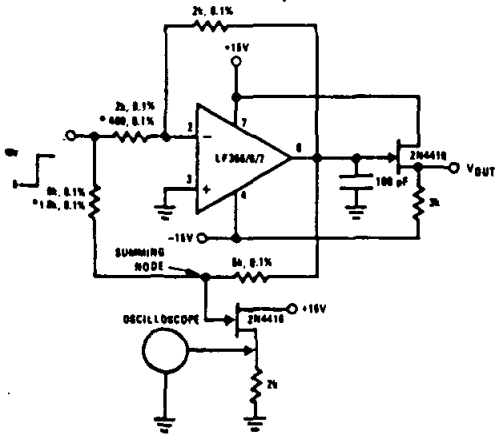


TL/H/5646-15

For distortion $\leq 1\%$ and a 20 Vp-p V_{OUT} swing power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

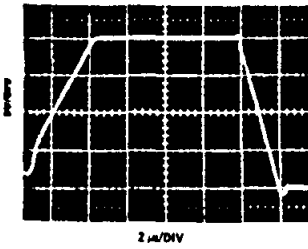


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

TL/H/5646-16

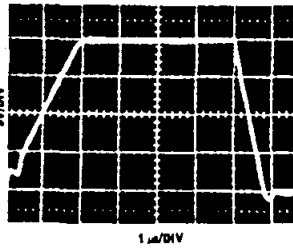
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



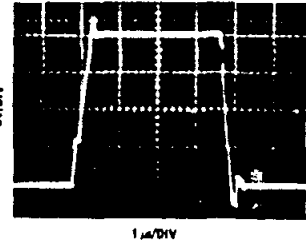
TL/H/5646-17

LF356



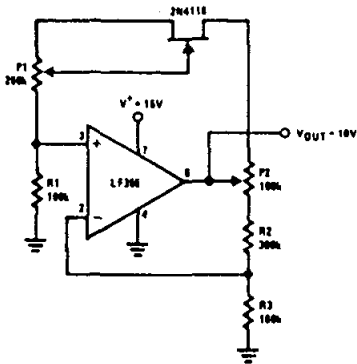
TL/H/5646-18

LF357



TL/H/5646-19

Low Drift Adjustable Voltage Reference

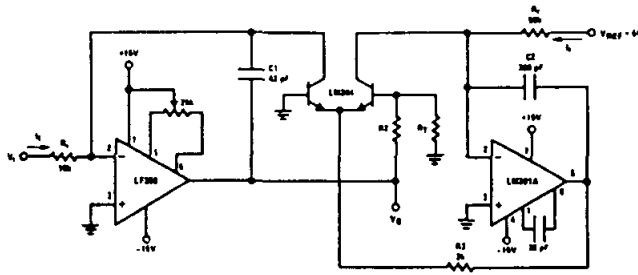


TL/H/5646-20

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}\text{C}$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
 - Low I_B
 - Low drift
 - Low supply current

Typical Applications (Continued)

Fast Logarithmic Converter

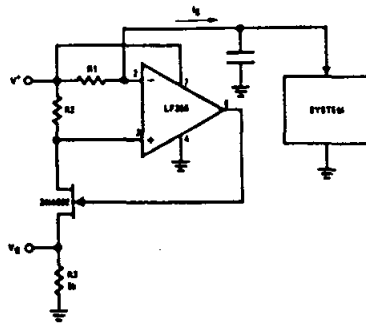


TL/H/5646-21

- Dynamic range: $100 \mu\text{A} < I_i < 1 \text{ mA}$ (5 decades), $|V_{O}| = 1\text{V/decade}$
- Transient response: $3 \mu\text{s}$ for $\Delta I_i = 1 \text{ decade}$
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T : Tel Labs type Q81 + 0.3%/°C

$$|V_{out}| = \left[1 + \frac{R_2}{R_T} \right] \frac{KT}{q} \ln V_i \left[\frac{R_T}{V_{REF} R_1} \right] = \log V_i \frac{1}{R_1 V_T} R_2 = 15.7k, R_T = 1k, 0.3\%/^{\circ}\text{C (for temperature compensation)}$$

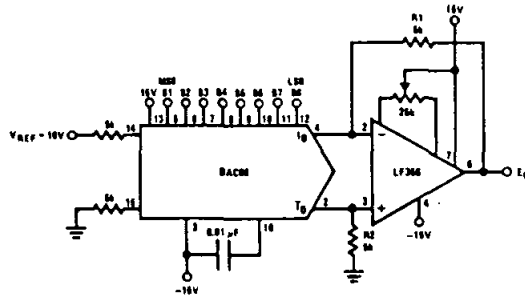
Precision Current Monitor



TL/H/5646-31

- $V_0 = 5 R_1/R_2 (V/\text{mA of } I_i)$
- R1, R2, R3: 0.1% resistors
- Use LF155 for
 - Common-mode range to supply range
 - Low I_B
 - Low V_{OS}
 - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



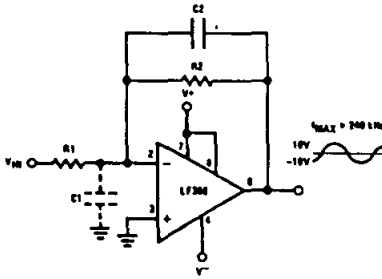
TL/H/5646-32

- R1, R2 should be matched within $\pm 0.05\%$
- Full-scale response time: $3 \mu\text{s}$

E_0	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
-0.040	0	1	1	1	1	1	1	1	(-) Zero-Scale
-9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Typical Applications (Continued)

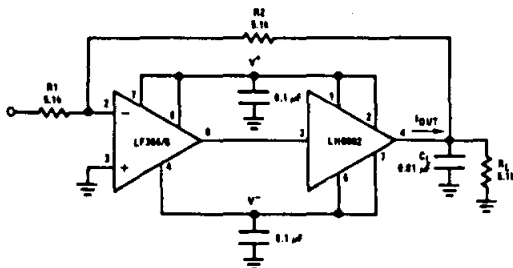
Wide BW Low Noise, Low Drift Amplifier



• Power BW: $f_{MAX} = \frac{S_r}{2\pi V_p} \approx 240 \text{ kHz}$

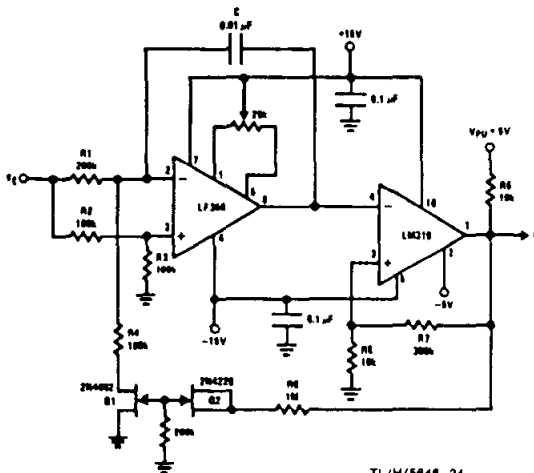
- Parasitic input capacitance C_1 (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} = 150 \text{ mA}$ (will drive $R_L \geq 100 \Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}} \text{ V}/\mu\text{s}$ (with C_L shown)
- No additional phase shift added by the current amplifier

3 Decades VCO

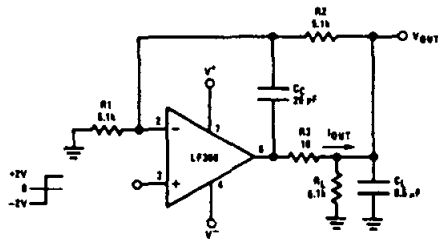


TL/H/5646-24

$$f = \frac{V_C (R_8 + R_7)}{(8 V_{PI} R_8 R_1) C} \quad 0 \leq V_C = 30\text{V}, 10 \text{ Hz} \sim 10 \text{ kHz}$$

- R_1, R_4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads

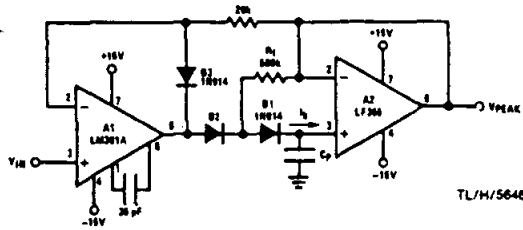


- Overshoot 6%
- $t_d \approx 10 \mu\text{s}$
- When driving large C_L , the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} = \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s} \text{ (with } C_L \text{ shown)}$$

TL/H/5646-22

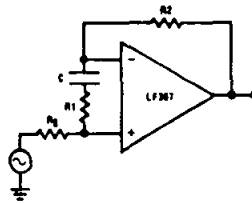
Low Drift Peak Detector



TL/H/5646

- By adding D_1 and R_1 , $V_{D1} = 0$ during hold mode. Leakage of D_2 provided by feedback path through R_1 .
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_p .
- Diode D_3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D_2 .
- Maximum input frequency should be $\ll \frac{1}{2} \pi R_1 C_{D2}$ where C_{D2} is the shunt capacitance of D_2 .

Non-Inverting Unity Gain Operation for LF157



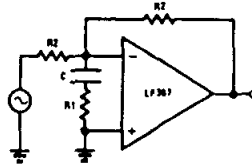
$$R_1 C \geq \frac{1}{(2\pi)(5 \text{ MHz})}$$

$$R_1 = \frac{R_2 + R_3}{4}$$

$$A_v(DC) = 1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

Inverting Unity Gain for LF157



$$R_1 C \geq \frac{1}{(2\pi)(5 \text{ MHz})}$$

$$R_1 = \frac{R_2}{4}$$

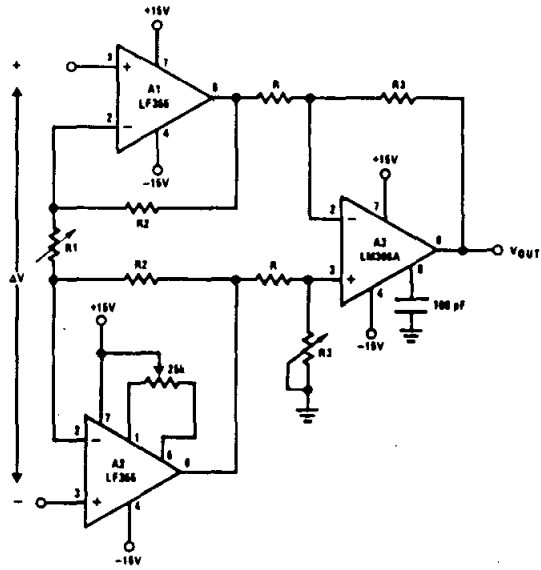
$$A_v(DC) = -1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

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Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier

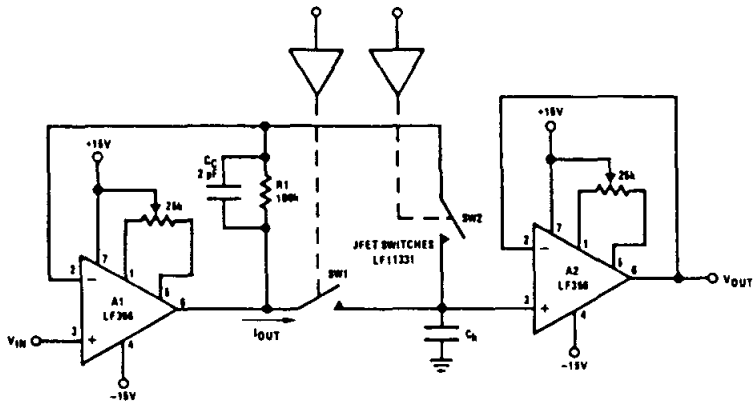


- $V_{OUT} = \frac{R3}{R} \left[\frac{2R2}{R1} + 1 \right] \Delta V, V^- + 2V \leq V_{IN \text{ common-mode}} \leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

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Typical Applications (Continued)

Fast Sample and Hold



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- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A , estimated by:

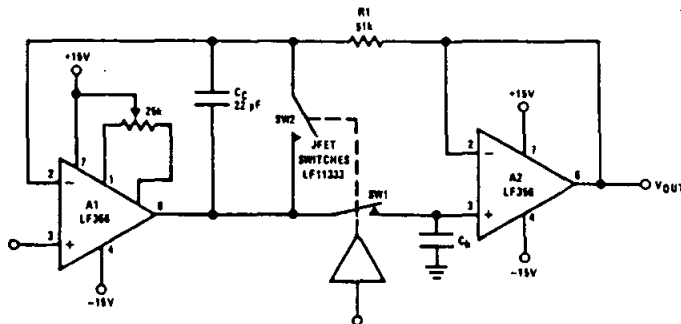
$$T_A \approx \left[\frac{2R_{ON} V_{IN} C_H}{S_T} \right]^{1/2} \text{ provided that:}$$

$$V_{IN} < 2\pi S_T R_{ON} C_H \text{ and } T_A > \frac{V_{IN} C_H}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \approx \frac{V_{IN} C_H}{20 \text{ mA}}$$

- LF156 develops full S_T output capability for $V_{IN} > 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

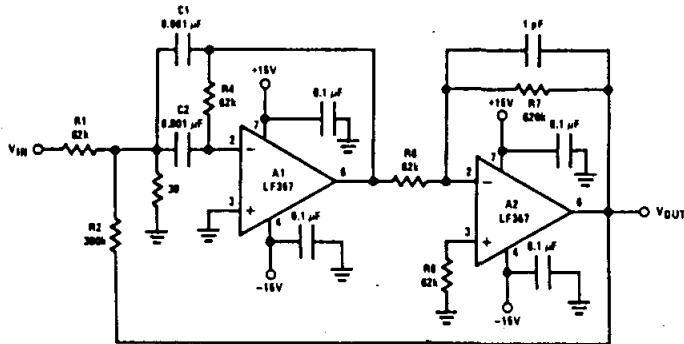


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- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_1 : additional compensation
- Use LF156 for
 - Fast settling time
 - Low V_{OS}

Typical Applications (Continued)

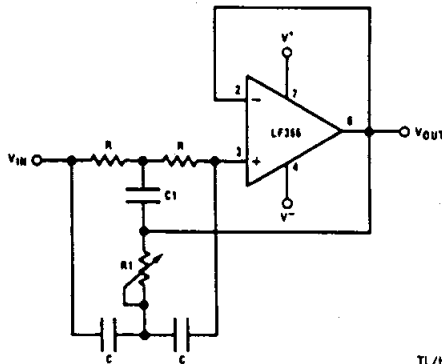
High Q Band Pass Filter



- By adding positive feedback (R2) Q increases to 40
- $f_{BP} = 100 \text{ kHz}$
- $\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

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High Q Notch Filter



- $2R1 = R = 10 \text{ M}\Omega$
- $2C = C1 = 300 \text{ pF}$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120 \text{ Hz}$, notch = -55 dB, $Q > 100$
- Use LF155 for
 - Low I_B
 - Low supply current

TL/H/5646-34

BIODATA

BIODATA



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Nirm : 94.7.003.31073.06041
Alamat : MASPATI V/72
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Tempat/Tanggal lahir : MAKASSAR, 27 MEI 1975
Agama : KATOLIK

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Lulus SD Bali, Ujung Pandang tahun 1988.

Lulus SMP Negeri 5, Ujung Pandang 1991.

Lulus SMA Sasana Bhakti, Surabaya tahun 1994.

Mahasiswa Universitas Katolik Widya Mandala Fakultas Teknik Jurusan Teknik Elektro, Surabaya, Angkatan 1994.