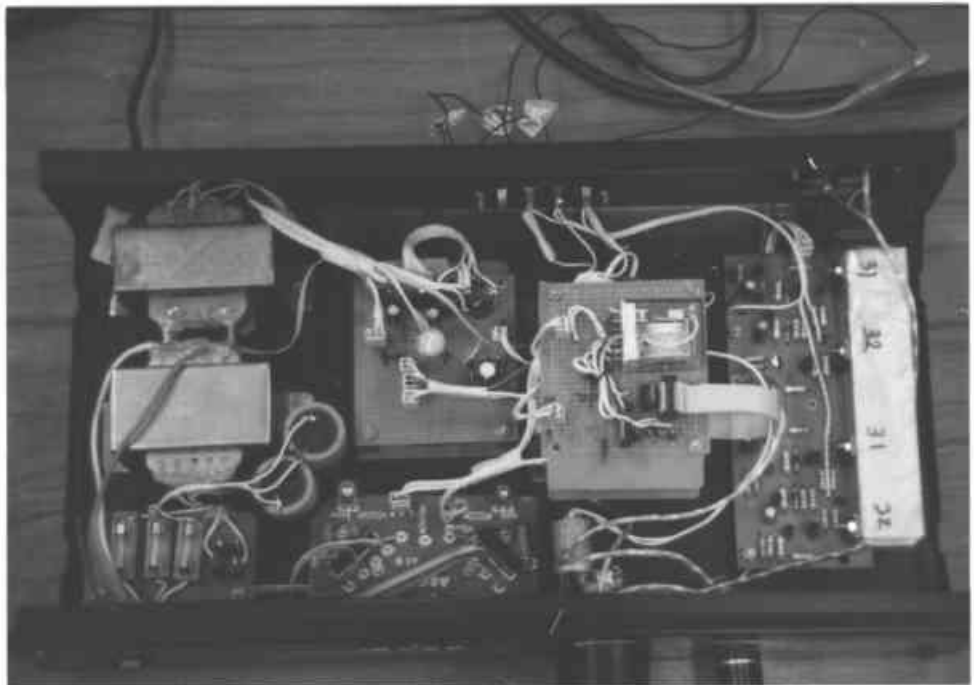
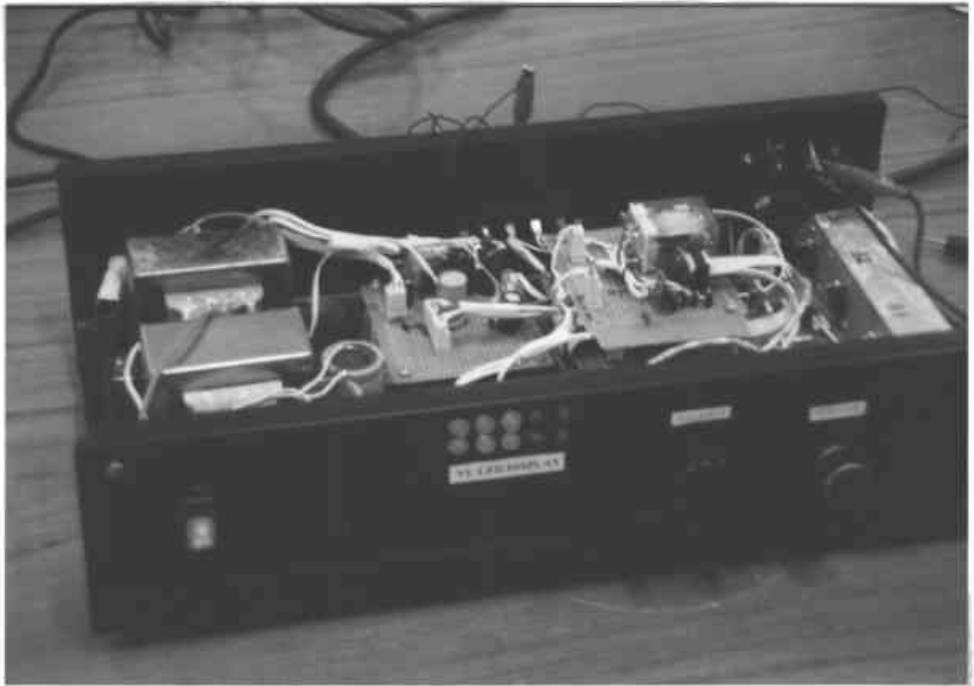
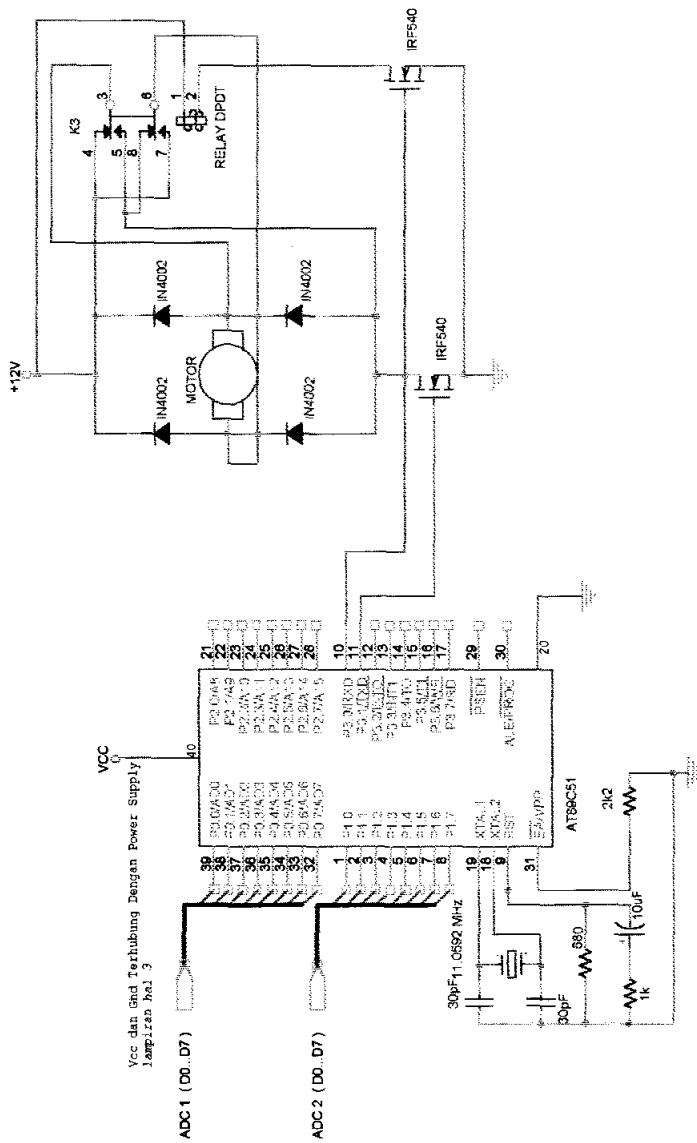


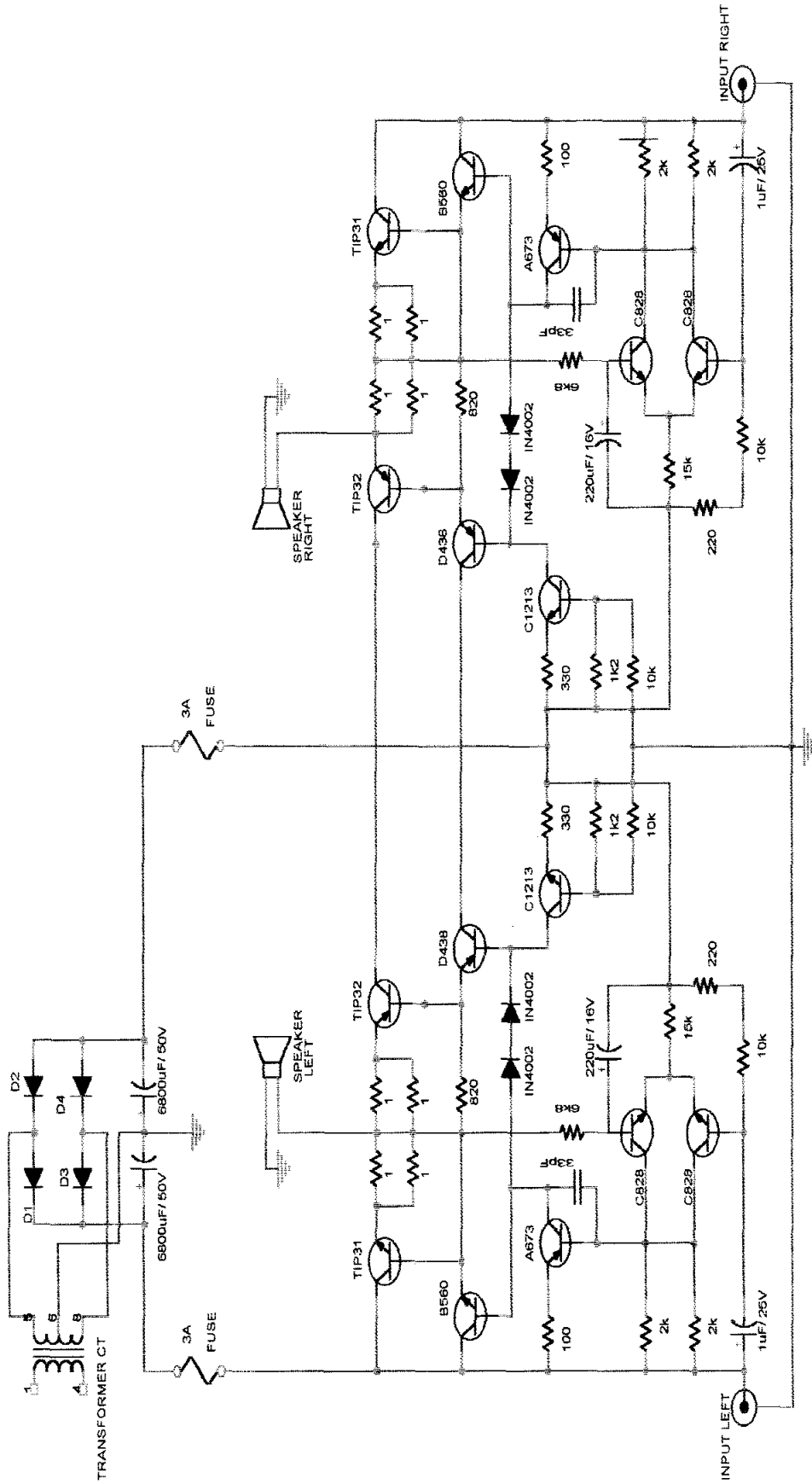
LAMPIRAN

FOTO ALAT KESELURUHAN

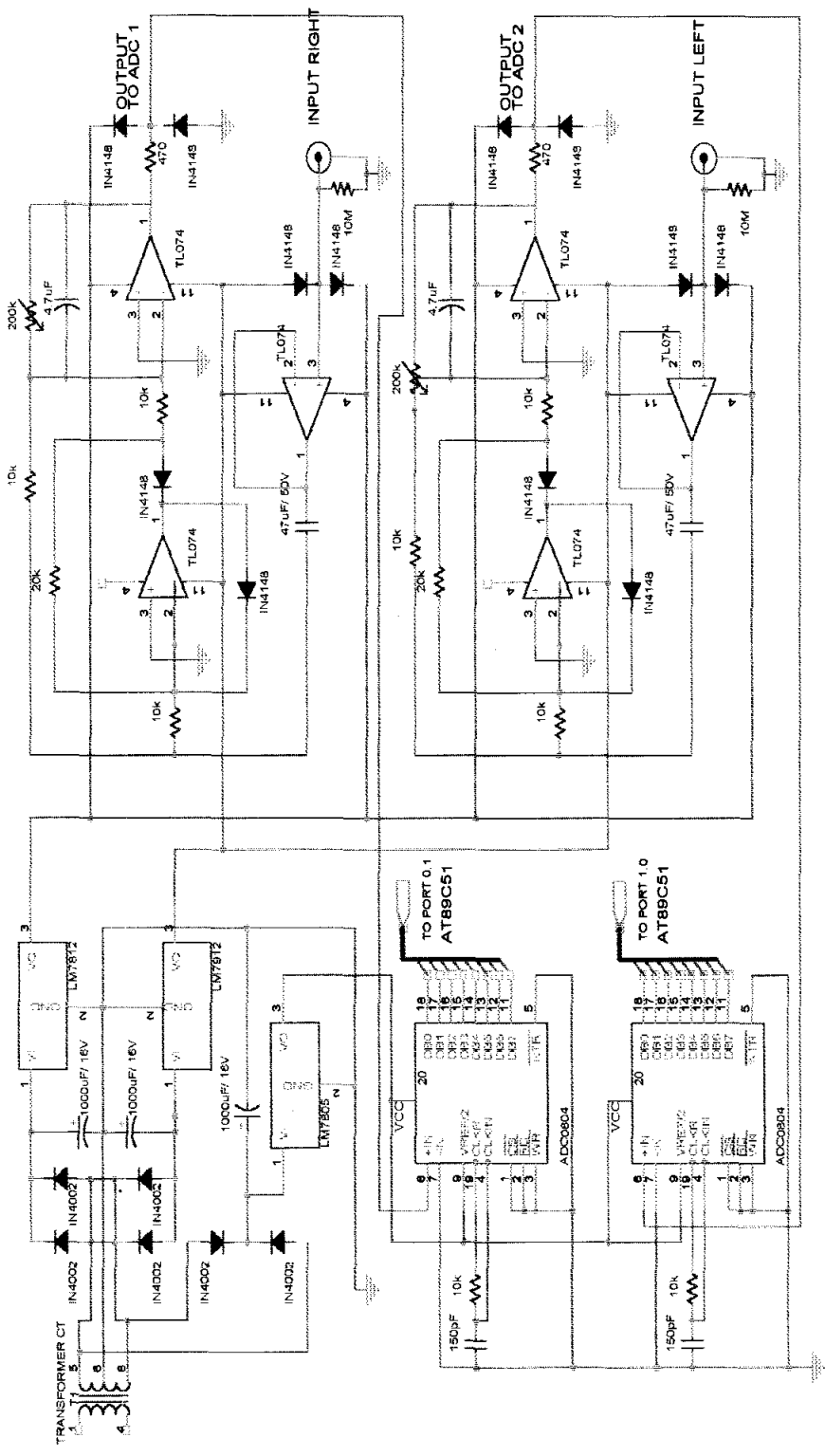




**RANGKAIAN MIKROKONTROLLER DENGAN
DRIVER MOTOR DC**



RANGKAIAN POWER AMPLIFIER DENGAN POWER SUPPLYNYA



**RANGKAIAN ADC DAN RPS
MENGUNAKAN POWER SUPPLY BERSAMA**

```

;-----
;   MAIN PROGRAM
;-----
MULAI          MOV  SP,#30H
ULANG          MOV  R2,#P0          (Input dari ADC 1 ke Port 0)

                MOV  A,#P1          (Input dari ADC 2 ke Port 1)
                SUBB A,R2          (ADC1 Dikurangi ADC2)

                JNC  KANAN          (pembanding putar kiri atau kanan)
                MOV  R2,A
                MOV  A,#255
                SUBB A,R2
                SETB P3.0          (Motor putar kiri)
                AJMP JALAN

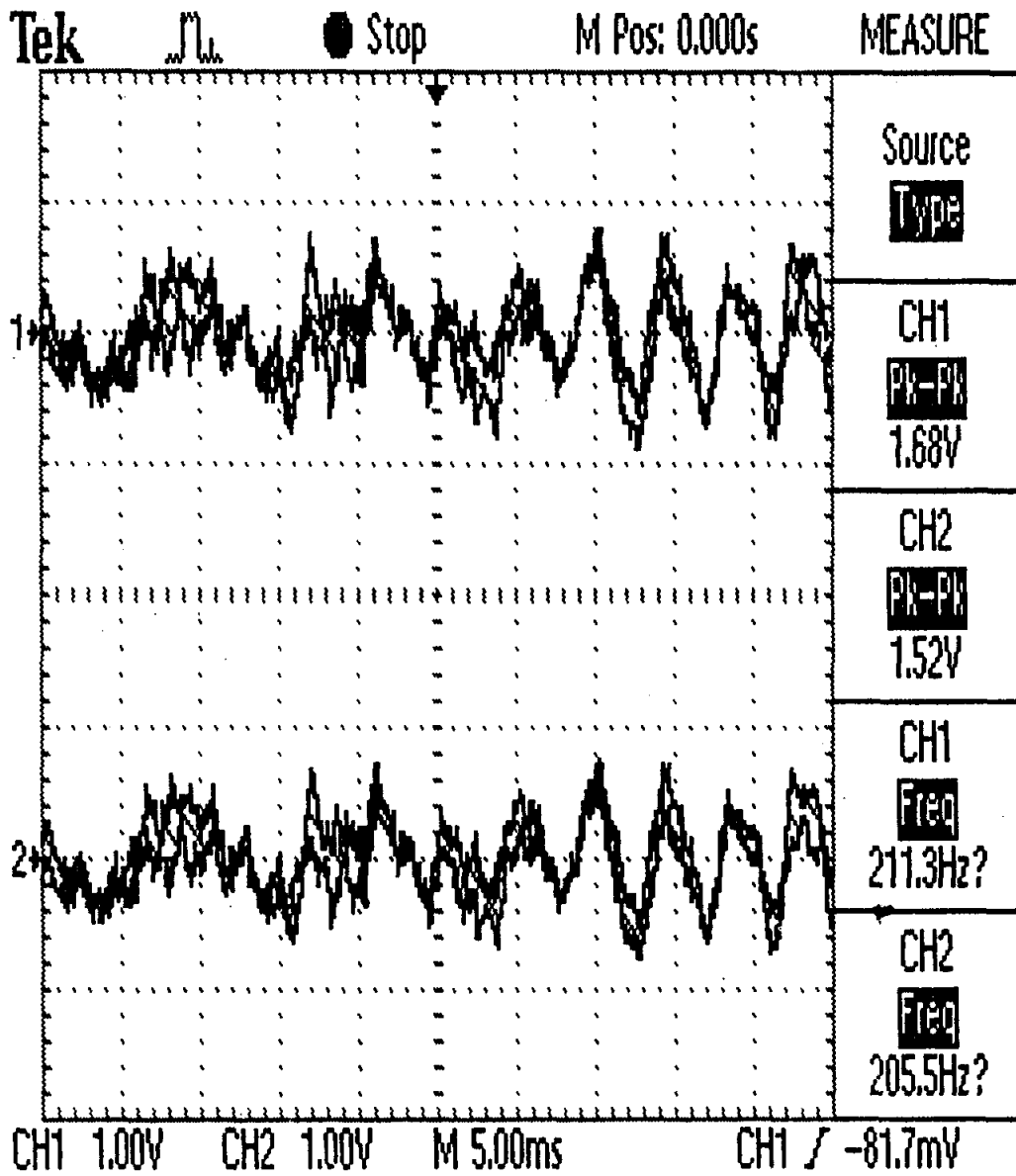
KANAN          CLR  P3.0          (motor putar kanan)
JALAN          CJNE A,#20,CEK_CARRY (Histerisis antara ADC1 dan
ADC2)
                AJMP STOP

CEK_CARRYJC   STOP
JALANI        SETB P3.1          (motor ON)
                AJMP ULANG

STOP          CLR  P3.1          (motor OFF)
                MOV  R6,#1
WAIT          MOV  R7,#200
                DJNZ R7,$
                DJNZ R6,WAIT
                AJMP ULANG

```

- Sinyal Audio (Input Tape)



INSTRUCTION DEFINITIONS

ACALL addr11**Function:** Absolute Call

Description: ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC, opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2k block of the program memory as the first byte of the instruction following ACALL. No flags are affected.

Example: Initially SP equals 07H. The label "SUBRTN" is at program memory location 0345 H. After executing the instruction,

ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain 25H and 01H, respectively, and the PC will contain 0345H.

Bytes: 2**Cycles:** 2**Encoding:****Operation:**

ACALL

 $(PC) \leftarrow (PC) + 2$ $(SP) \leftarrow (SP) + 1$ $(SP) \leftarrow (PC_{7-0})$ $(SP) \leftarrow (SP) + 1$ $(SP) \leftarrow (PC_{15-8})$ $(PC_{10-0}) \leftarrow \text{page address}$

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	rel	Jump if direct bit is set	3	24
JNB	rel	Jump if direct bit is not set	3	24
JBC	bit,rel	Jump if direct bit is set and clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	24
LCALL	addr16	Long subroutine call	3	24
RET		Return from subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute jump	2	24
LJMP	addr16	Long jump	3	24
SJMP	rel	Short jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is zero	2	24
JNZ	rel	Jump if Accumulator is not zero	2	24
CJNE	A,direct,rel	Compare direct byte to ACC and jump if not equal	3	24
CJNE	A,#data,rel	Compare immediate to ACC and jump if not equal	3	24
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ	Rn,rel	Decrement register and jump if not zero	2	24
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	24
NOP		No operation	1	12

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Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	RN,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to ACC	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to ACC	1	24
MOVX	A,@Ri	Move external RAM (8-bit addr) to ACC	1	24
MOVX	A,@DPTR	Move external RAM (16-bit addr) to ACC	1	24
MOVX	A,@Ri,A	Move ACC to external RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move ACC to external RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order digit indirect RAM with ACC	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to carry	2	24
ANL	C,/bit	AND complement of direct bit to carry	2	24
ORL	C,bit	OR direct bit to carry	2	24
ORL	C,/bit	OR complement of direct bit to carry	2	24
MOV	C,bit	Move direct bit to carry	2	12
MOV	bit,C	Move carry to direct bit	2	24
JC	rel	Jump if carry is set	2	24
JNC	rel	Jump if carry not set	2	24

80C51 FAMILY INSTRUCTION SET

Table 7. 80C51 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.							
Instructions that Affect Flag Settings ⁽¹⁾							
Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

⁽¹⁾Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn Register R7-R0 of the currently selected Register Bank.

direct 8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].

@Ri 8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.

#data 8-bit constant included in the instruction.

#data 16 16-bit constant included in the instruction

addr 16 16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.

addr 11 11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.

rel Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.

bit Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC	DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS			
ADD A,Rn	Add register to Accumulator	1	12
ADD A,direct	Add direct byte to Accumulator	2	12
ADD A,@Ri	Add indirect RAM to Accumulator	1	12
ADD A,#data	Add immediate data to Accumulator	2	12
ADDC A,Rn	Add register to Accumulator with carry	1	12
ADDC A,direct	Add direct byte to Accumulator with carry	2	12
ADDC A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC A,#data	Add immediate data to ACC with carry	2	12
SUBB A,Rn	Subtract Register from ACC with borrow	1	12
SUBB A,direct	Subtract direct byte from ACC with borrow	2	12
SUBB A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB A,#data	Subtract immediate data from ACC with borrow	2	12
INC A	Increment Accumulator	1	12
INC Rn	Increment register	1	12

BIODATA

Nama Lengkap : **FX. TONY. SETIAWAN**
NRP : 5103095030
NIRM : 94.7.003.31073.06029
Tempat ,Tanggal lahir : Lasem, November 1975
Agama : Katolik
Alamat Rumah : Jl Raya Timur 162
Jatirogo-Tuban

Riwayat Pendidikan :

- SDN Wotsogo I Jatirogo-Tuban, lulus tahun 1988
- SMPK Santo Yusup 2, Malang, lulus tahun 1991
- SMAK Santa Agnes, Surabaya , lulus tahun 1995
- Universitas Katolik Widya Mandala Fakultas Teknik Jurusan Teknik Elektro, Surabaya , angkatan 1995

