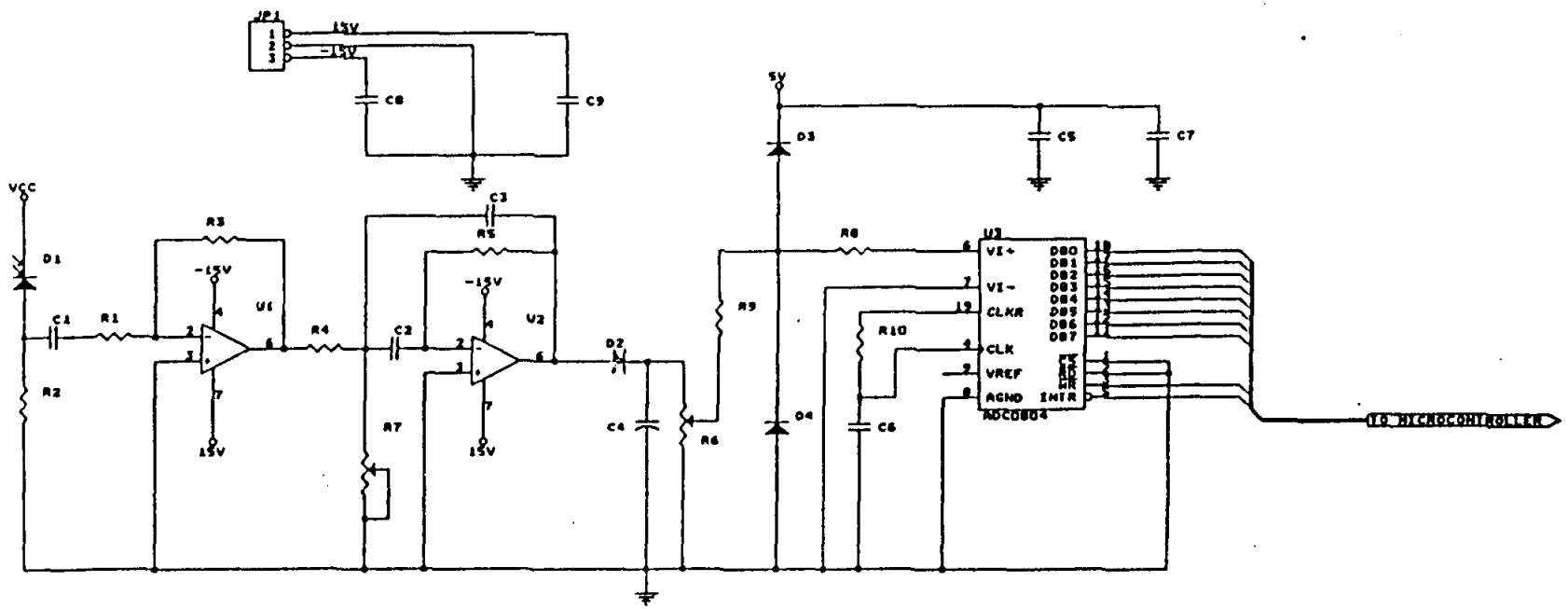
LAMPIRAN A

RANGKAIAN SKEMATIK



Size	Document Number	REV
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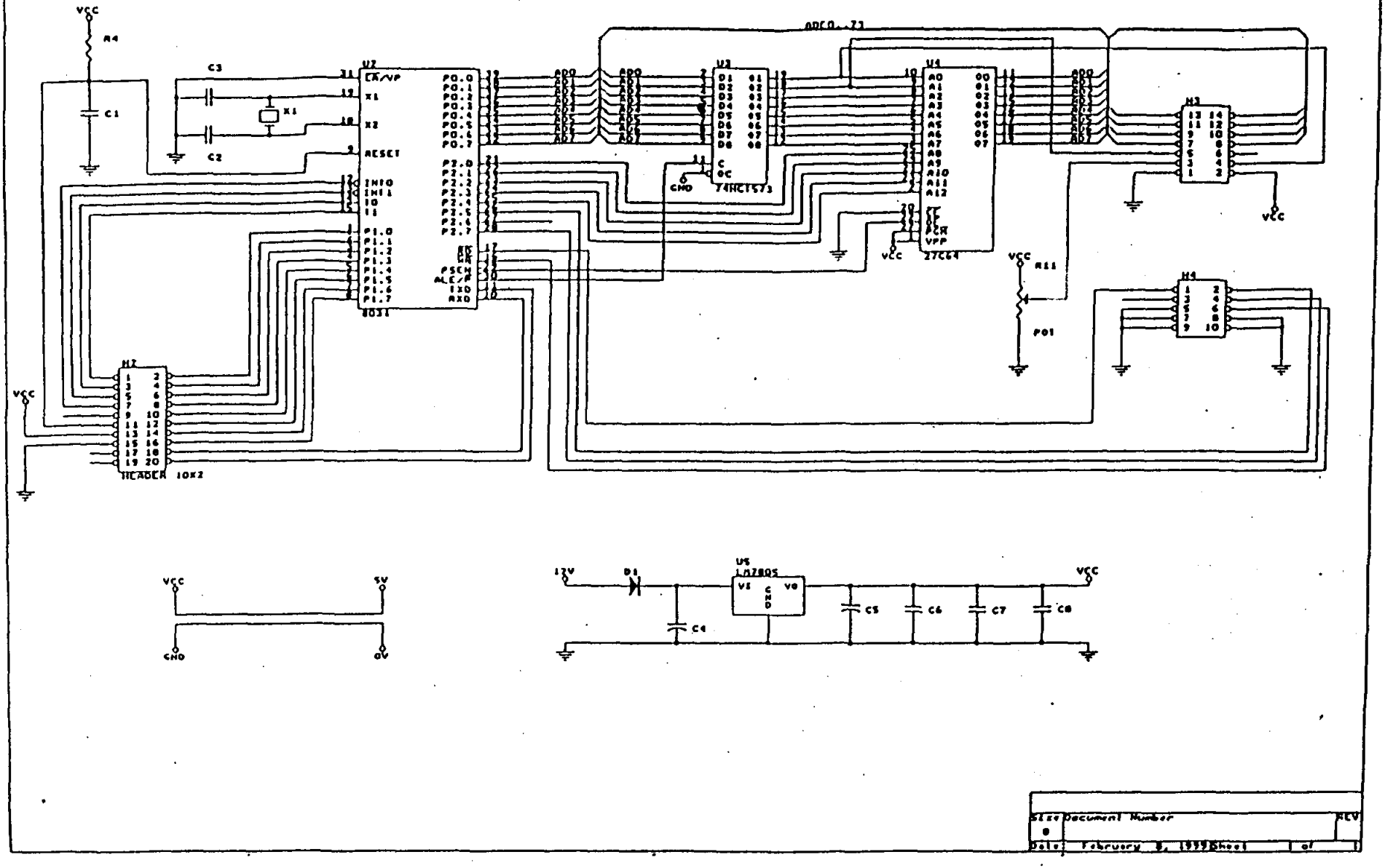
Date: February 9, 1999	Sheet 1 of 1	

DAFTAR KOMPONEN
GAMBAR RANGKAIAN I

C1 = 10 nF
C2 = 1 nF
C3 = 1 nF
C4 = 10 nF
C5 = 100 nF
C6 = 10 nF
C7 = 100 nF
C8 = 100 nF
C9 = 100 nF

D1 = 1N4148
D2 = 1N4148
D3 = 1N4148
D4 = 1N4148

R1 = 22 KΩ
R2 = 47 KΩ
R3 = 4,7 MΩ
R4 = 47 KΩ
R5 = 1 MΩ
R6 = 100 KΩ
R7 = 5 KΩ
R8 = 470 Ω
R9 = 470 Ω
R10 = 10 KΩ


VCC
R4
C1
C3
C2
X1
U2
80C31
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
RESET
PSEN
ALE/P
TXD
RXD
U3
74HCT573
U4
27C64
ADC0..7
J3
J4
R11
P01
J2
HEADER 10X2
5V
GND
0V
12V
D1
U5
LM7805
VI
VO
C4
C5
C6
C7
C8
Size
Document Number
REV
Date: February 8, 1999
Sheet
of

DAFTAR KOMPONEN
GAMBAR RANGKAIAN II

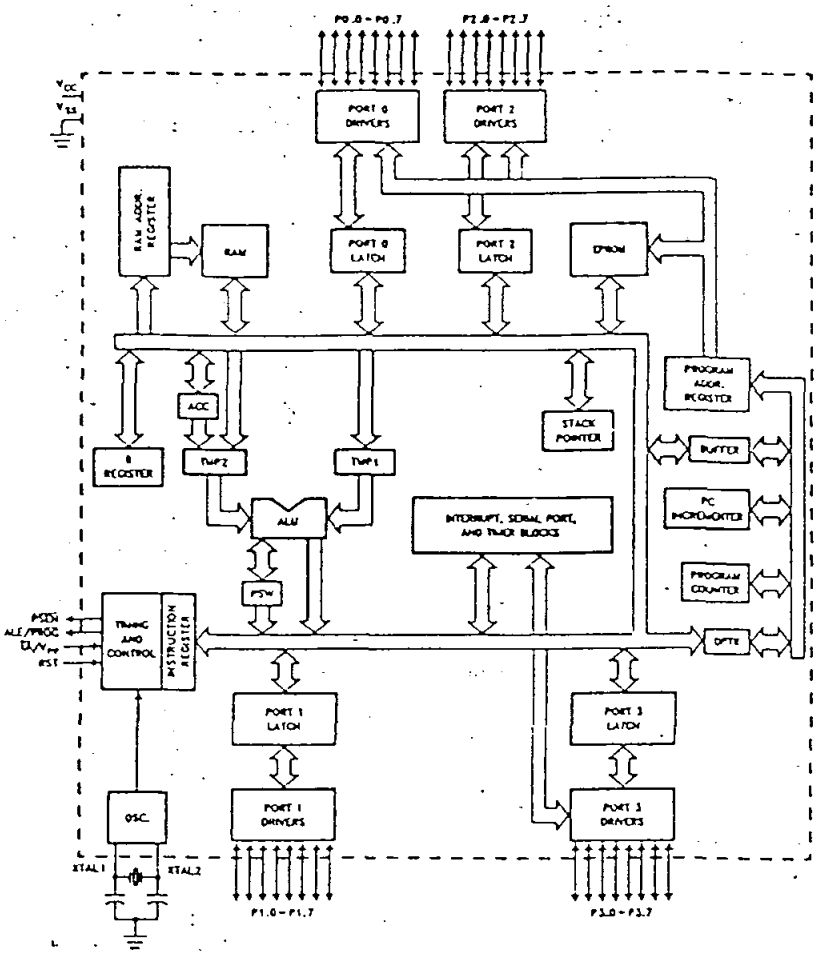
C1 = 10 µF
C2 = 22 pF
C3 = 22 pF
C4 = 2200 µF / 25 Volt
C5 = 1000 µF / 16 Volt
C6 = 100 nF
C7 = 100 nF
C8 = 100 nF

D1 = 1N4148

R4 = 10 KΩ
R11 = 100 KΩ
X1 = 14 MHz

8751BH
SINGLE-CHIP 8-BIT MICROCOMPUTER WITH 4K BYTES OF EPROM PROGRAM MEMORY

- Program Memory Lock
- 128 Bytes Data Ram
- Quick Pulse Programming™ Algorithm
- 12.75 Volt Programming Voltage
- Boolean Processor
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Programmable Serial Channel
- 64K External Program Memory Space
- 64K External Data Memory Space



270248-1

Figure 1. 8751BH Block Diagram

September 1988
Order Number: 270248-003

PACKAGES

Part	Prefix	Package Type
8751BH	P	40-Pin Plastic DIP
	N	44-Pin PLCC

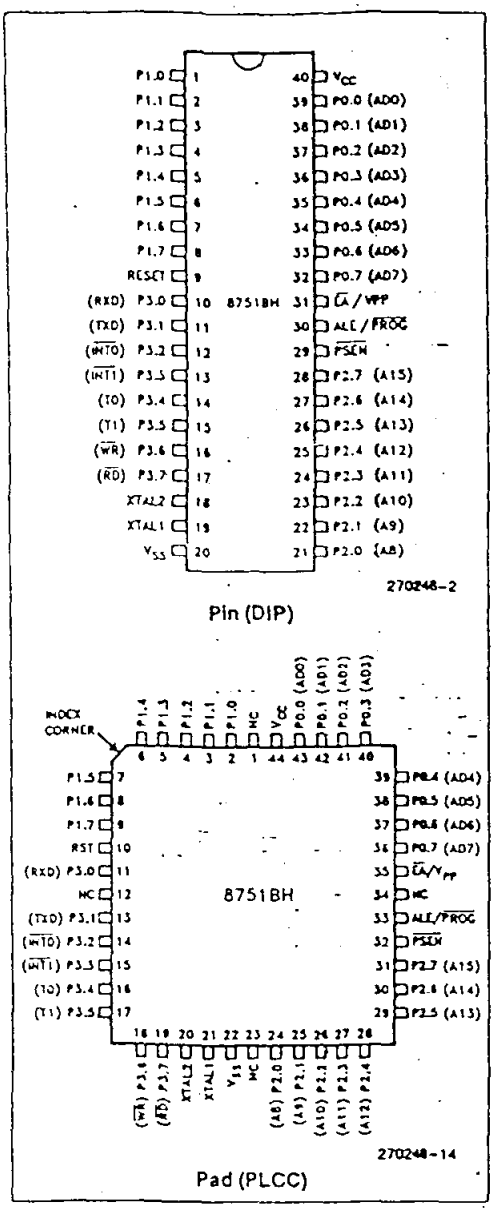


Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS®-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory.

When the 87518H is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Applications Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

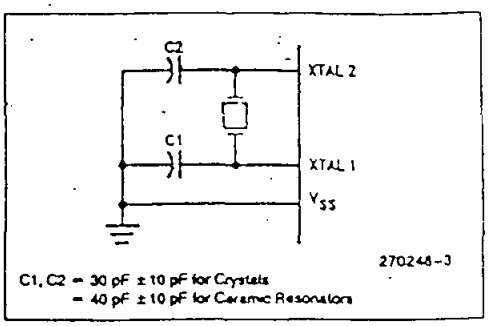


Figure 3. Oscillator Connections

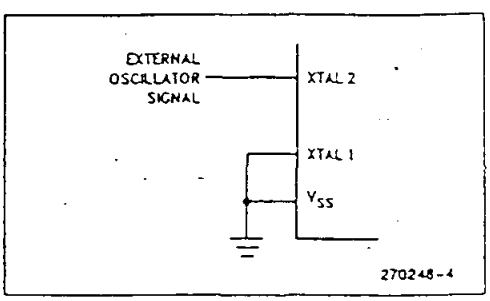


Figure 4. External Clock Drive Configuration

DESIGN CONSIDERATIONS

If an 87518H is replacing an 8751H in an existing design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the V_{IH} and I_{IH} specifications for the EA pin differ significantly between the 8751H and 87518H.

SOLUTE MAXIMUM RATINGS*

pient Temperature Under Bias ....0°C to +70°C
rage Temperature .....−65°C to +150°C
tage on $\overline{EA}$/V_{PP} Pin to V_{SS} ...−0.5V to +13.0V
tage on Any Other Pin to V_{SS} ....−0.5V to +7V
ximum I_{OL} Per I/O Pin .....15 mA
wer Dissipation.....1.5W
sed on PACKAGE heat transfer limitations, not
ice power consumption)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V)

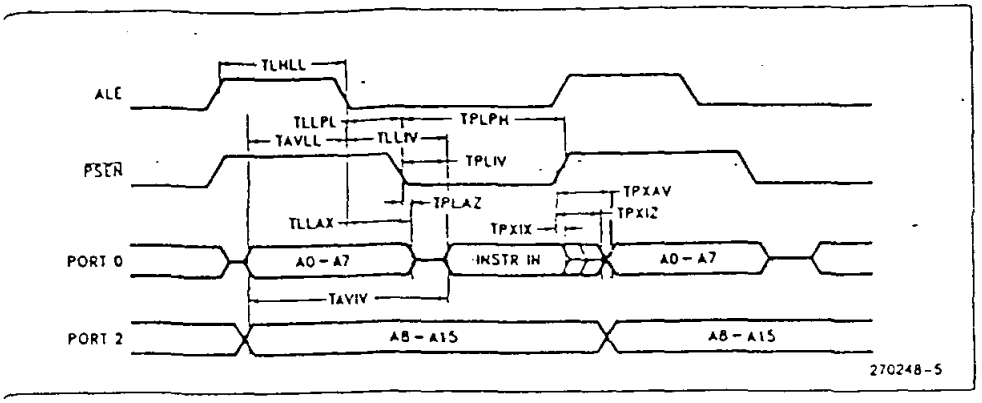
ymbol	Parameter	Min	Max	Unit	Test Conditions
IL	Input Low Voltage (Except $\overline{EA}$)	−0.5	0.8	V	
IL1	Input Low Voltage $\overline{EA}$	V_{SS}	0.7	V	
IH	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	2.0	V_{CC}+0.5	V	
IH1	Input High Voltage XTAL2, RST	2.5	V_{CC}+0.5	V	XTAL1 = VSS
IH2	Input High Voltage to $\overline{EA}$	4.5	5.5	V	
OL	Output Low Voltage (Note 3) (Ports 1, 2 and 3)		0.45	V	I_{OL} = 1.6 mA (Note 1)
OL1	Output Low Voltage (Note 3) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)		0.45	V	I_{OL} = 3.2 mA (Notes 1, 2)
OH	Output High Voltage (Ports 1, 2, 3, ALE/$\overline{PROG}$ and $\overline{PSEN}$)	2.4		V	I_{OH} = −80 μA
OH1	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −400 μA
IL	Logical 0 Input Current (Ports 1, 2, 3 and RST)		−1	mA	V_{IN} = 0.45V
IL1	Logical 0 Input Current ($\overline{EA}$)		−10	mA	V_{IN} = VSS
IL2	Logical 0 Input Current (XTAL2)		−3.2	mA	V_{IN} = 0.45 V XTAL1 = V_{SS}
LI	Input Leakage Current (Port 0)		±10	μA	0.45 < V_{IN} < V_{CC}
IH	Logical 1 Input Current ($\overline{EA}$)		1	mA	4.5V < V_{IN} < 5.5V
IH1	Input Current to RST to Activate Reset		500	μA	V_{IN} < (V_{CC} − 1.5V)
CC	Power Supply Current		175	mA	All Outputs Disconnected
CIO	Pin Capacitance		10	pF	Test Freq = 1MHz

OTES:
. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE/$\overline{PROG}$ nd Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins ake 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the LE/$\overline{PROG}$ pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address atch with a Schmitt Trigger STROBE input.
. ALE/$\overline{PROG}$ refers to a pin on the 8751BH. ALE refers to a timing signal that is output on the ALE/$\overline{PROG}$ pin.
. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port -
Port 0: 26 mA
Ports 1, 2, and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
. If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater han the listed test conditions.

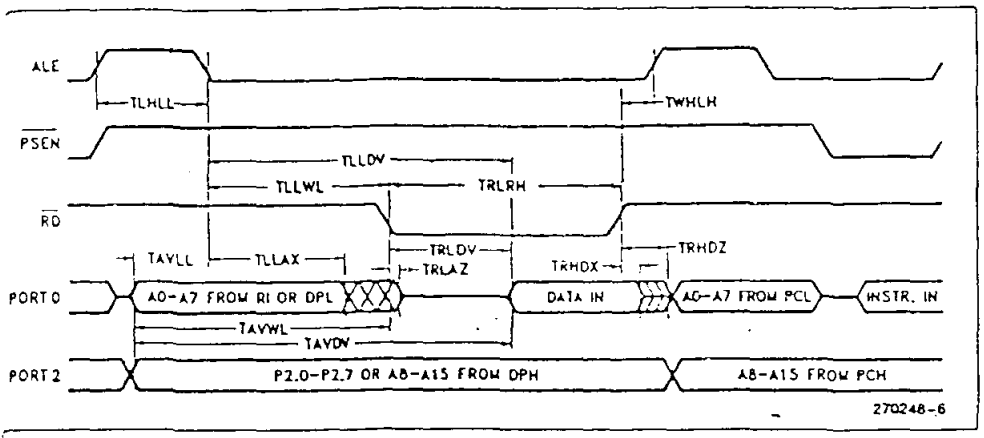
A.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

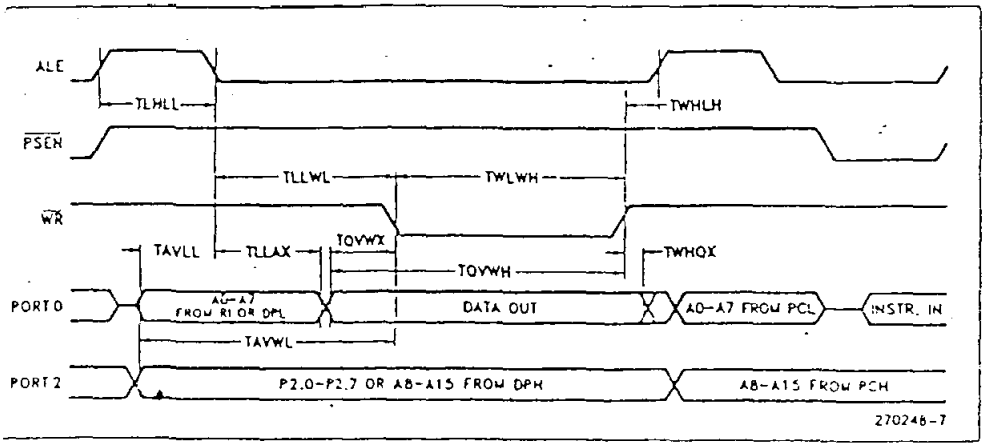
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instruction In		233		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL−35		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		125		3TCLCL−125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		63		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instruction In		302		5TCLCL−115	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		TCLCL−60		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TWHQX	Data Held After $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns



External Program Memory Read Cycle



External Data Memory Read Cycle

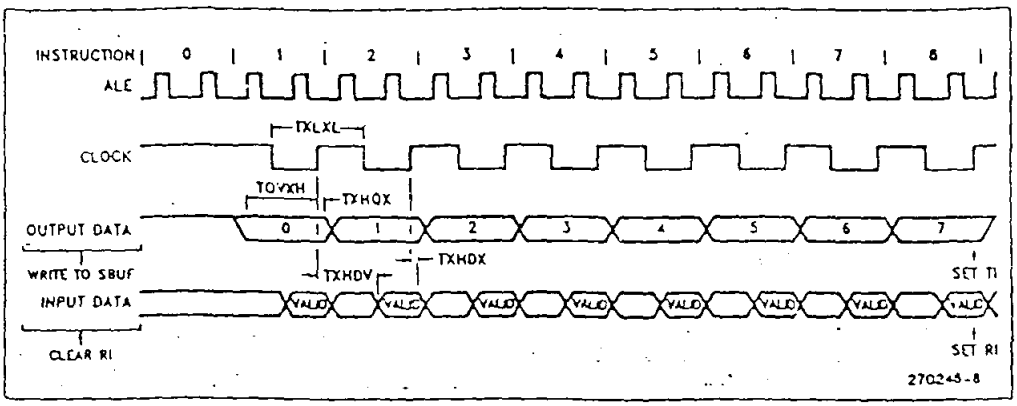


External Data Memory Write Cycle

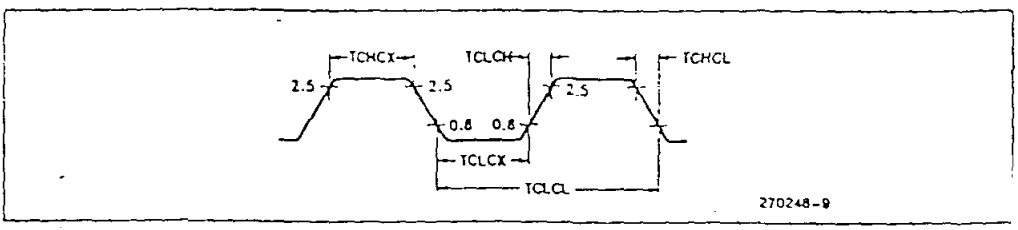
SERIAL PORT TIMING — SHIFT REGISTER MODE

TEST CONDITIONS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance = 80 pF)

Symbol	Parameter	12MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−117		ns
TXHQX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns



Shift Register Mode Timing Waveforms

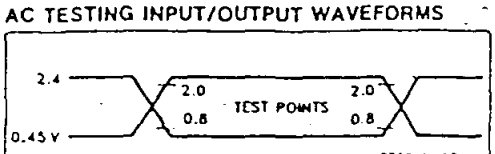


External Clock Drive Waveforms

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC TESTING INPUT/OUTPUT WAVEFORMS



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

EPROM CHARACTERISTICS

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, and RST, $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 1. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally $\overline{EA}/V_{PP}$ is held at a logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. *The V_{PP} source should be well regulated and* free of glitches.

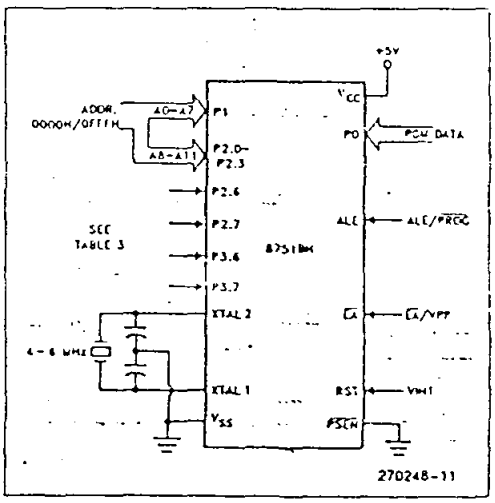


Figure 5. Programming the EPROM

Table 1. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/VPP	P2.7	P2.6	P3.6	P3.7
Program Code Data	1	0	0*	VPP	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program Encryption Table Use Addresses 0-1FH	1	0	0*	VPP	1	0	0	1
Program Lock x = 1	1	0	0*	VPP	1	1	1	1
Bits (LBx) x = 2	1	0	0*	VPP	1	1	0	0
Read Signature	1	0	1	1	0	0	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
"VPP" = +12.75V ±0.25V
* ALE/PROG is pulsed low for 100 uS for programming. (Quick-Pulse Programming™)

QUICK-PULSE PROGRAMMING™ ALGORITHM

The 8751BH can be programmed using the Quick-Pulse Programming Algorithm for microcontrollers. The features of the new programming method are a lower VPP (12.75 volts as compared to 21 volts) and a shorter programming pulse. It is possible to program the entire 4K Bytes of EPROM memory in less than 13 seconds with this algorithm.

To program the part using the new algorithm, VPP must be 12.75 ±0.25 Volts. ALE/PROG is pulsed low for 100 μseconds, 25 times. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 1. The only difference in programming Lock features is that the Lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

PROGRAM VERIFICATION

If the Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.3. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation. (If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.)

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active low read strobe.

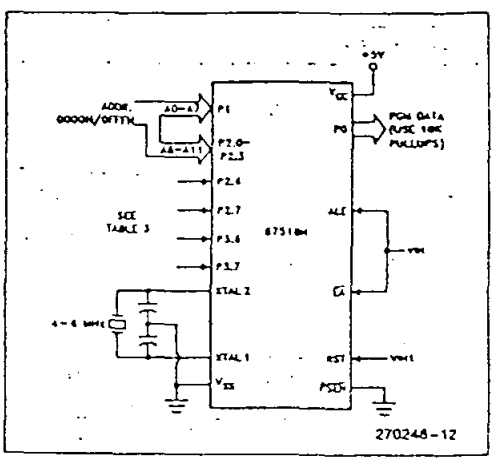


Figure 6. Verifying the EPROM

PROGRAM MEMORY LOCK

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form.

It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bits

Also included in the EPROM Program Lock scheme are two Lock Bits which function as shown in Table 2.

Table 2. Lock Bits and their Features

Lock Bits		Logic Enabled
LB1	LB2	
U	U	Minimum Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array)
P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled
P	P	Same as above, but Verify is also disabled
U	P	Reserved for Future Definition

P = Programmed
U = Unprogrammed

To ensure proper functionality of the chip, the internally latched value of the $\overline{EA}$ pin must agree with its external state.

ERASURE CHARACTERISTICS

This device is in a plastic package without a window and, therefore, cannot be erased.

Reading the Signature Bytes

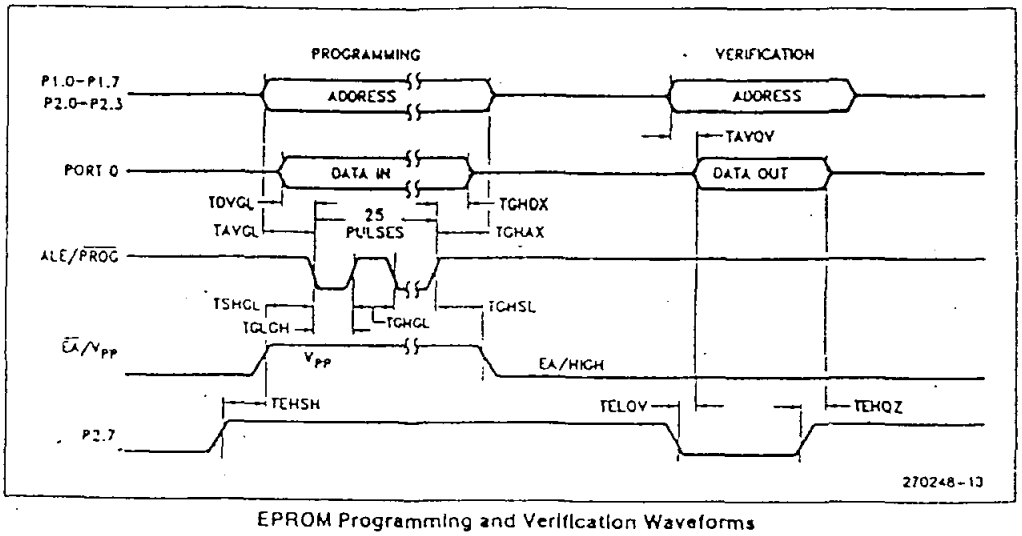
The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. the values returned are:

(030H) = 89H indicates manufactured by Intel
(031H) = 51H indicates 8751BH

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C, V_{CC} = 5.0V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
IPP	Programming Supply Current		50	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µsec
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		µsec
TGLGH	$\overline{PROG}$ Width	90	110	µsec
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µsec



EPROM Programming and Verification Waveforms

National Semiconductor Corporation

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

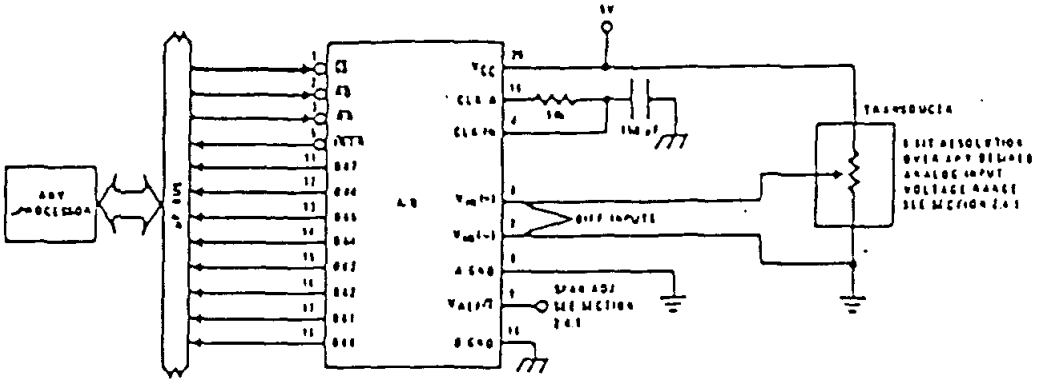
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

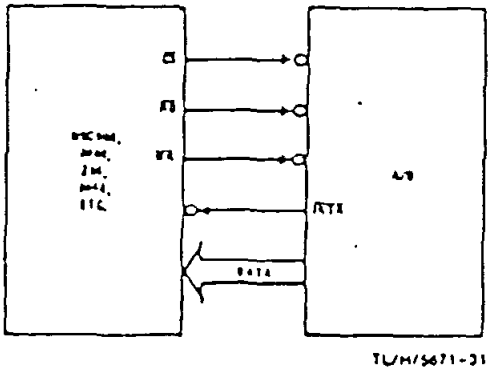
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671-1

8080 Interface



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Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ± 10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(WR)}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
$V_{IN}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	$I_{OUT} = 1.6\ mA$, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0\ mA$, $V_{CC} = 4.75\ V_{DC}$			0.4 0.4	V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640\ kHz$, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

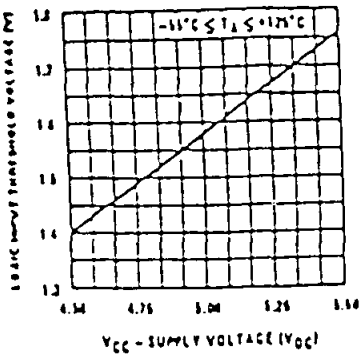
Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

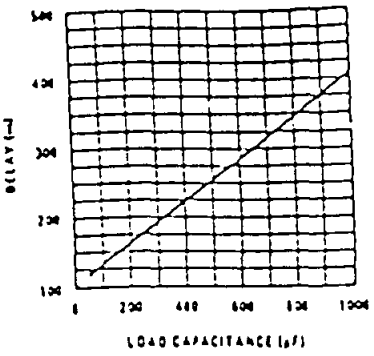
Note 9: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each resistor is 1k. Total ladder input resistance is the sum of the two equal resistors.

Typical Performance Characteristics

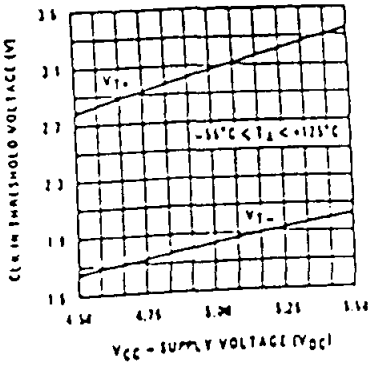
Logic Input Threshold Voltage vs. Supply Voltage



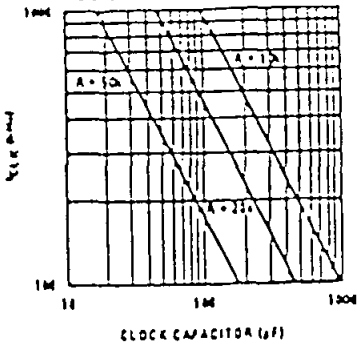
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



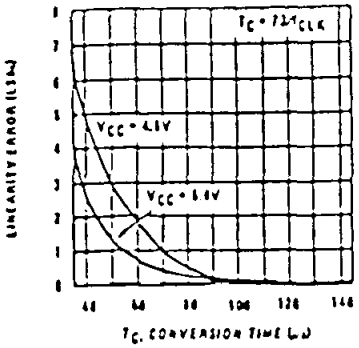
CLK IN Schmitt Trip Levels vs. Supply Voltage



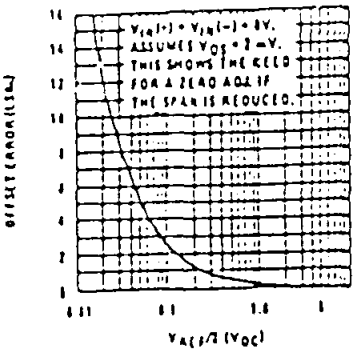
f_{CLK} vs. Clock Capacitor



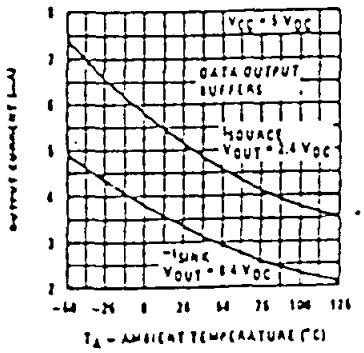
Full-Scale Error vs Conversion Time



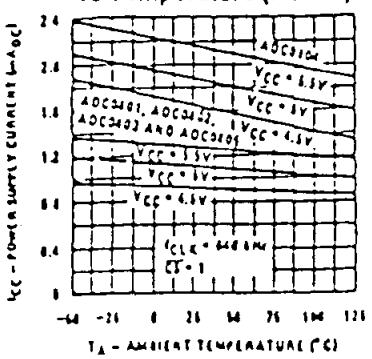
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



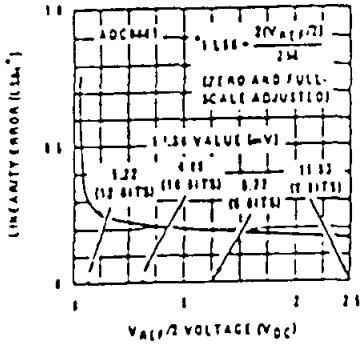
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



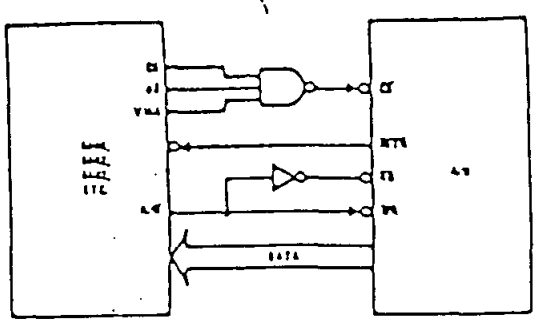
Linearity Error at Low $V_{REF}/2$ Voltages



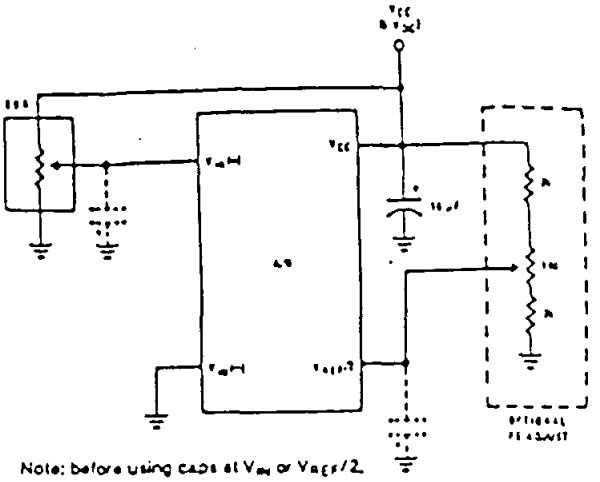
TL/H/5671-2

Typical Applications (Continued)

6800 Interface

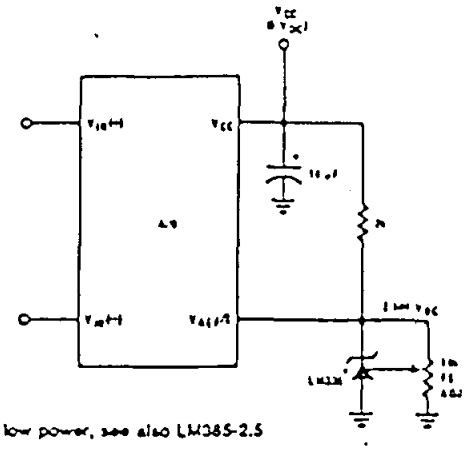


Ratiometric with Full-Scale Adjust



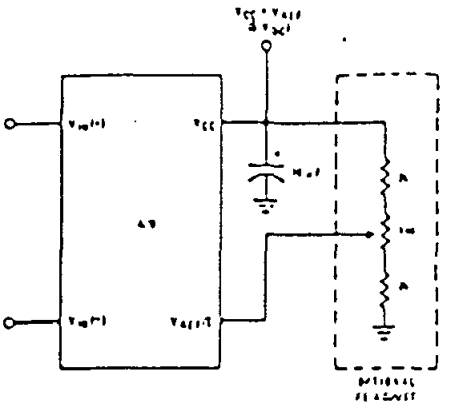
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

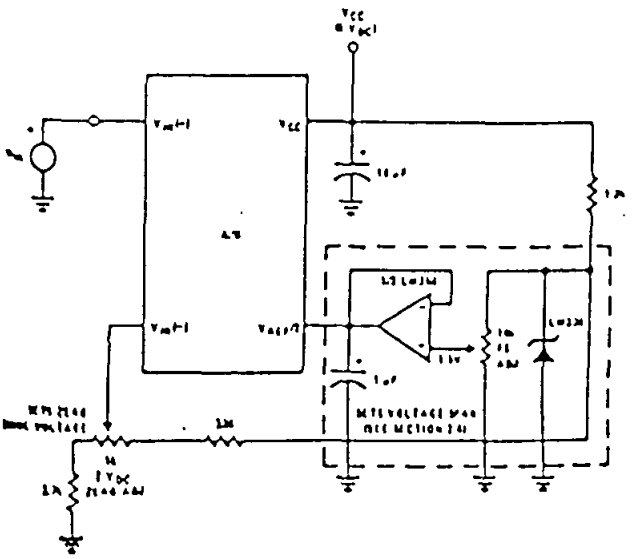


*For low power, see also LM385-2.5

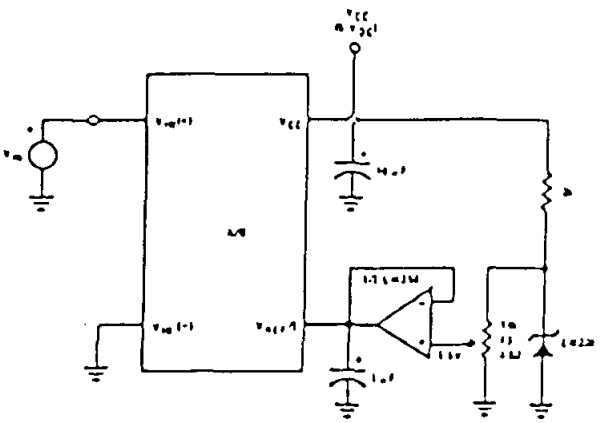
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

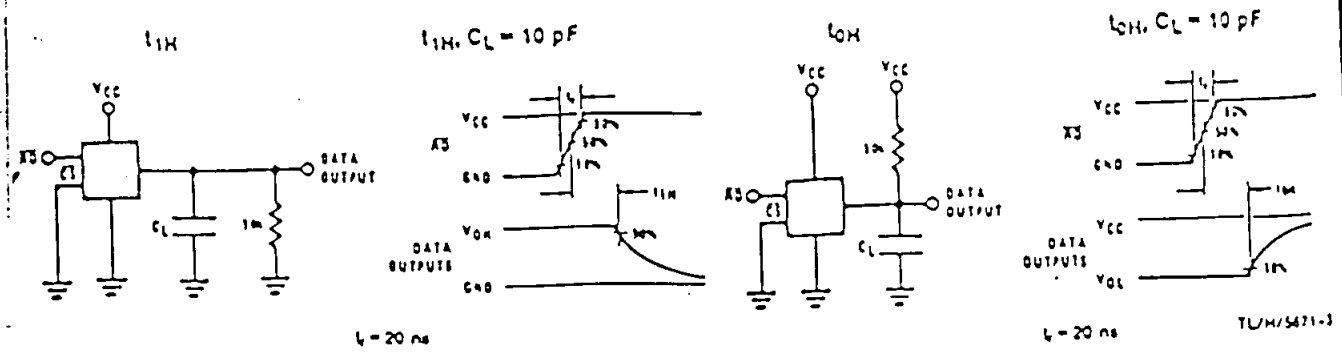


Span Adjust: $0V \leq V_{IN} \leq 3V$

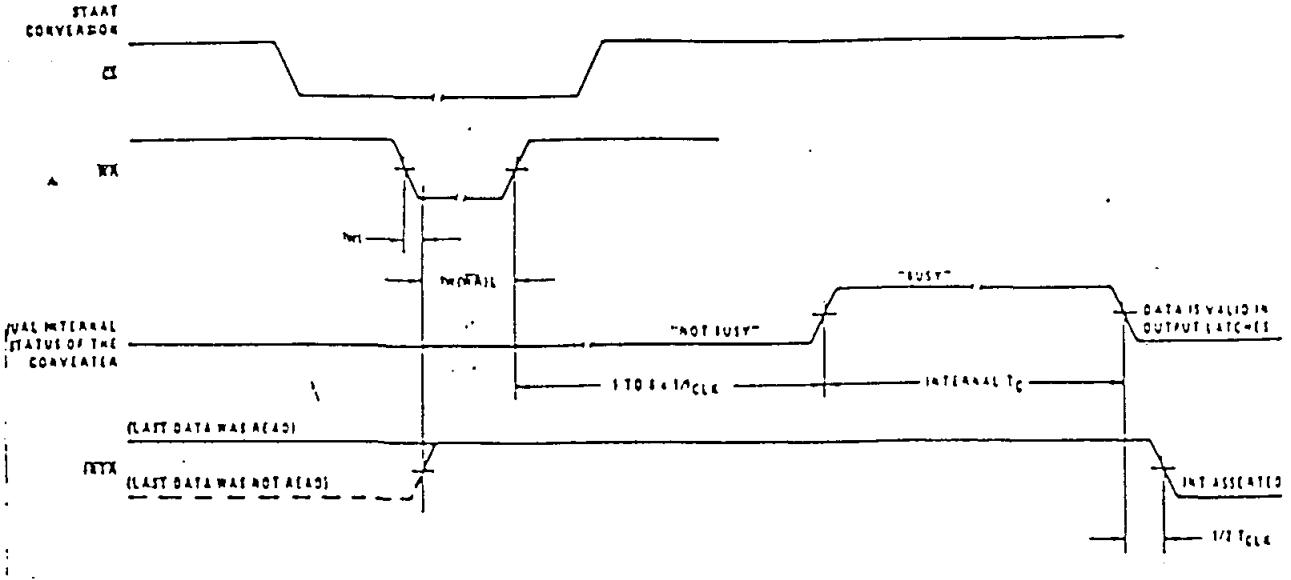


TL/H/5671-5

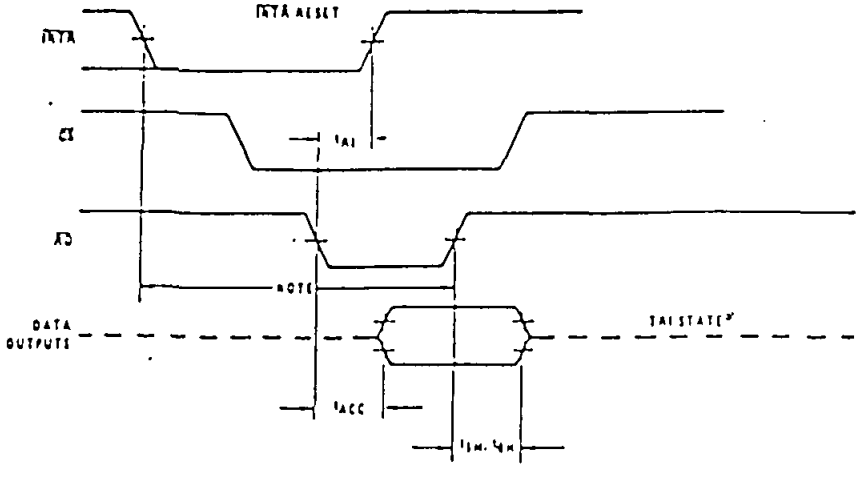
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$



Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

TL/H/5671-4

LAMPIRAN B

PERANGKAT LUNAK

```
WR_CTRL_REG         EQU 2000H      % Inisialisasi prosesor 87C51 &
WR_DATA_REG         EQU 2001H        LCD %
RD_CTRL_REG         EQU 2002H
RD_DATA_REG         EQU 2003H
TIME_DELAY          EQU 21H
DSP1                EQU 22H
DSP2                EQU 23H
DSP3                EQU 24H
DSP4                EQU 25H
BUFFER              EQU 28H
INPUT               EQU 29H
PRINT_COUNTER       EQU 30H


                    ORG 0000H
                    AJMP MAIN

                    ORG 100H

MAIN:               MOV SP,#70H
                    ACALL INIT_LCD

                    MOV A,#00001100B
                    ACALL CTRL_OUT

LOGO:               ACALL CLEAR_DISPLAY  % mencetak header logo %
                    ACALL PRT_TITLE1
                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY
                    ACALL PRT_TITLE2
                    ACALL DELAY_5S

                    ACALL CLEAR_DISPLAY

MEASURE:            ACALL READ_P1        % membaca ADC dan
                    MOV BUFFER,INPUT       menampilkan di LCD %
                    ACALL TOTAL_RESULT
                    ACALL DELAY_2S
                    SJMP MEASURE

READ_P1:            PUSH DPH             % membaca pada Port P1 %
                    PUSH DPL
                    MOV A,P1
                    MOV INPUT,A

                    CLR C
                    SUBB A,#3
                    JNC REAL_DISP
                    MOV INPUT,#0
                    SJMP EXIT_RD_P1

REAL_DISP:          MOV A,#255
                    SUBB A,INPUT
                    MOV INPUT,A
```

```
                    CLR C
                    SUBB A,#200
                    JC LOW_DISP

HIGH_DISP:          SJMP EXIT_RD_P1

LOW_DISP:           MOV A,INPUT
                    MOV B,#6
                    DIV AB
                    MOV INPUT,A
EXIT_RD_P1:         POP DPL
                    POP DPH
                    RET

TOTAL_RESULT:       PUSH DPH            % mencetak hasil
                    PUSH DPL              pengukuran di LCD %

                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#OUTPUT
                    ACALL OUT_CHAR

                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#OUTPUT2
                    ACALL OUT_CHAR

                    MOV R7,#5
                    ACALL LOCATE2
                    MOV A,DSP3
                    ACALL DATA_OUT

                    MOV R7,#6
                    ACALL LOCATE2
                    MOV A,DSP2
                    ACALL DATA_OUT

                    MOV R7,#7
                    ACALL LOCATE2
                    MOV A,DSP1
                    ACALL DATA_OUT

                    POP DPL
                    POP DPH
                    RET

PRT_TITLE1:         PUSH DPH            % mencetak Header 1 %
                    PUSH DPL
                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#HEADER1
                    ACALL OUT_CHAR
                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#HEADER2
                    ACALL OUT_CHAR
```

```
                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY

                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#HEADER3
                    ACALL OUT_CHAR
                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#HEADER4
                    ACALL OUT_CHAR

                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY

                    POP DPL
                    POP DPH
                    RET

PRT_TITLE2:         PUSH DPH            % mencetak header 2 %
                    PUSH DPL

                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#HEADER5
                    ACALL OUT_CHAR
                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#HEADER6
                    ACALL OUT_CHAR

                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY

                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#HEADER7
                    ACALL OUT_CHAR
                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#HEADER8
                    ACALL OUT_CHAR

                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY

                    POP DPL
                    POP DPH
                    RET
```

```
INIT_LCD:           PUSH DPH            % inisialisasi LCD %
                    PUSH DPL
                    PUSH PSW
                    PUSH ACC
                    MOV R0,#0FFH
                    ACALL DELAY_LOOP
                    MOV A,#00111000B
                    ACALL CTRL_OUT
                    MOV R0,#50H
                    ACALL DELAY_LOOP
                    MOV A,#00111000B
                    ACALL CTRL_OUT
                    MOV R0,#50H
                    ACALL DELAY_LOOP
                    MOV A,#00111000B
                    ACALL CTRL_OUT
                    MOV A,#00111000B
                    ACALL CTRL_OUT
                    MOV A,#00001000B
                    ACALL CTRL_OUT
                    MOV A,#00000001B
                    ACALL CTRL_OUT
                    MOV A,#00000110B
                    ACALL CTRL_OUT
                    POP ACC
                    POP PSW
                    POP DPL
                    POP DPH
                    RET

DELAY_LOOP:         PUSH DPH
                    PUSH DPL
DEL_LOOP:           DEC R0
                    NOP
                    NOP
                    NOP
                    CJNE R0,#0H,DEL_LOOP
                    POP DPL
                    POP DPH
                    RET

CLEAR_DISPLAY:      PUSH DPH            % membersihkan layar %
                    PUSH DPL
                    MOV A,#00000001B
                    ACALL CTRL_OUT
                    MOV R0,#0FFH
                    ACALL DELAY_LOOP
                    POP DPL
                    POP DPH
                    RET

DELAY_5S:           PUSH DPH            % delay 5 detik %
                    PUSH DPL
                    PUSH ACC
                    PUSH PSW
```

```
DEL1:           MOV A,#0FFH
DEL2:           MOV B,#0FFH
                DJNZ B,$
                DJNZ ACC,DEL2
                DJNZ R5,DEL3
                POP PSW
                POP ACC
                POP DPL
                POP DPH
                RET

DELAY_2S:       PUSH DPH            % delay 2 detik %
                PUSH DPL
                PUSH ACC
                PUSH PSW
                MOV R5,#06H
DEL3:           MOV A,#0FFH
DEL4:           MOV B,#0FFH
                DJNZ B,$
                DJNZ ACC,DEL4
                DJNZ R5,DEL3
                POP PSW
                POP ACC
                POP DPL
                POP DPH
                RET

DELAY_1S:       PUSH DPH            % delay 1 detik %
                PUSH DPL
                PUSH ACC
                PUSH PSW
                MOV R5,#03H
DEL5:           MOV A,#0FFH
DEL6:           MOV B,#0FFH
                DJNZ B,$
                DJNZ ACC,DEL6
                DJNZ R5,DEL5
                POP PSW
                POP ACC
                POP DPL
                POP DPH
                RET

DELAY:          PUSH DPH
                PUSH DPL
                PUSH ACC
                PUSH PSW
                MOV R5,TIME_DELAY
DEL7:           MOV A,#0FFH
DEL8:           MOV B,#0FFH
                DJNZ B,$
                DJNZ ACC,DEL8
                DJNZ R5,DEL7
                POP PSW
                POP ACC
                POP DPL
```

```
                    POP DPH
                    RET

HEADER1             DB 'MICROCONTROLLER ' % Karakter yang akan
dicetak di LCD %
HEADER2             DB '     DRIVEN     '
HEADER3             DB ' DIGITAL IODIUM '
HEADER4             DB '    TESTER      '
HEADER5             DB '  DESIGNED BY:  '
HEADER6             DB '  ANGKA WIJAYA  '
HEADER7             DB '   FTE  UNIKA   '
HEADER8             DB '  WIDYA MANDALA '
OUTPUT              DB ' IODIUM CONTAIN '
OUTPUT2             DB '         ppm    '

                    END
```

LAMPIRAN C

TABEL INSTRUKSI LCD

2.4 Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
(1) Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
(4) Display ON / OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
(6) Function Set	0	0	0	0	1	DL	1	*	*	*	Sets interface data length (DL)	40 µs
(7) CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
(8) DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

* : Invalid bit
A_{CG} : CG RAM address
A_{DD} : DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

Table 3 Correspondence between character codes and character patterns

Upper bit 4 bit / Lower bit 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)												
××××0001	(2)												
××××0010	(3)												
××××0011	(4)												
××××0100	(5)												
××××0101	(6)												
××××0110	(7)												
××××0111	(8)												
××××1000	(1)												
××××1001	(2)												
××××1010	(3)												
××××1011	(4)												
××××1100	(5)												
××××1101	(6)												
××××1110	(7)												
××××1111	(8)												

FOTO ALAT

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