LAMPIRAN

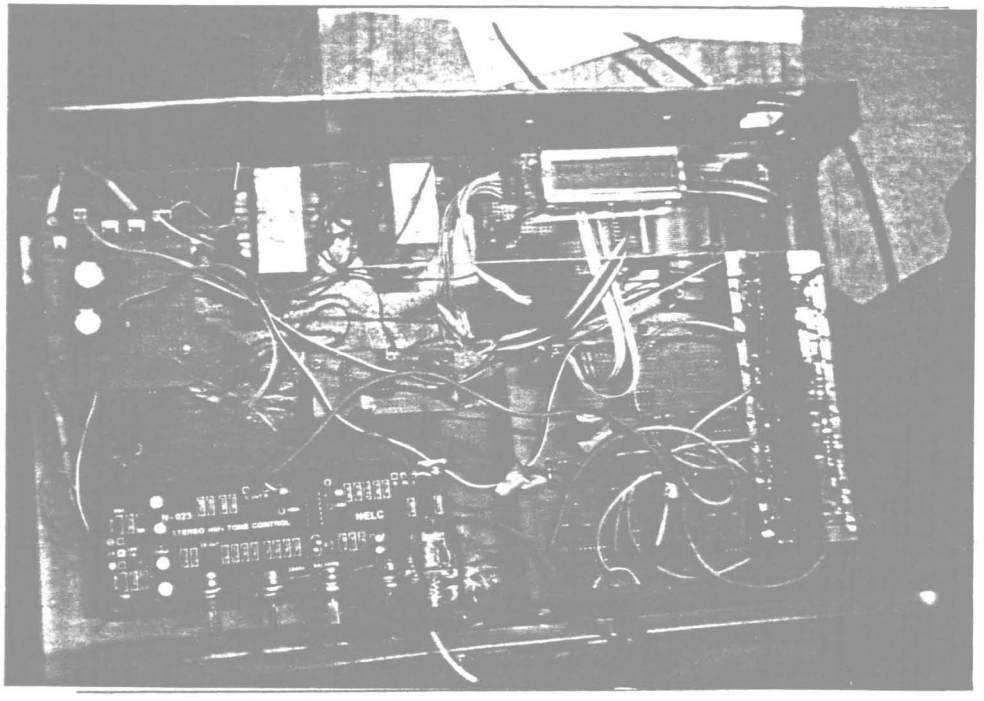
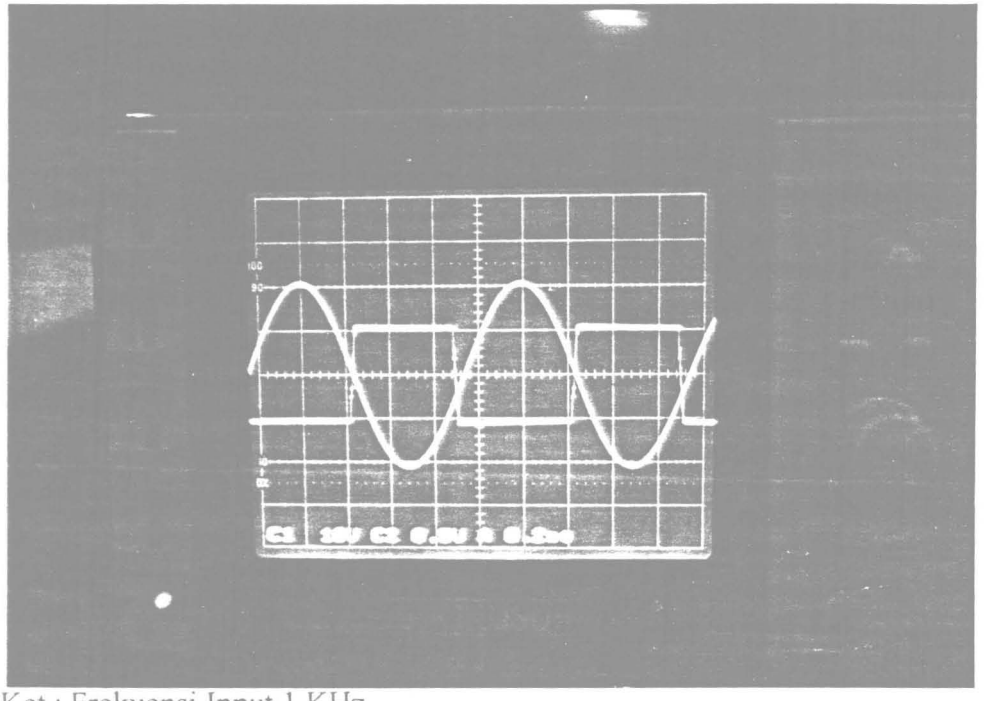
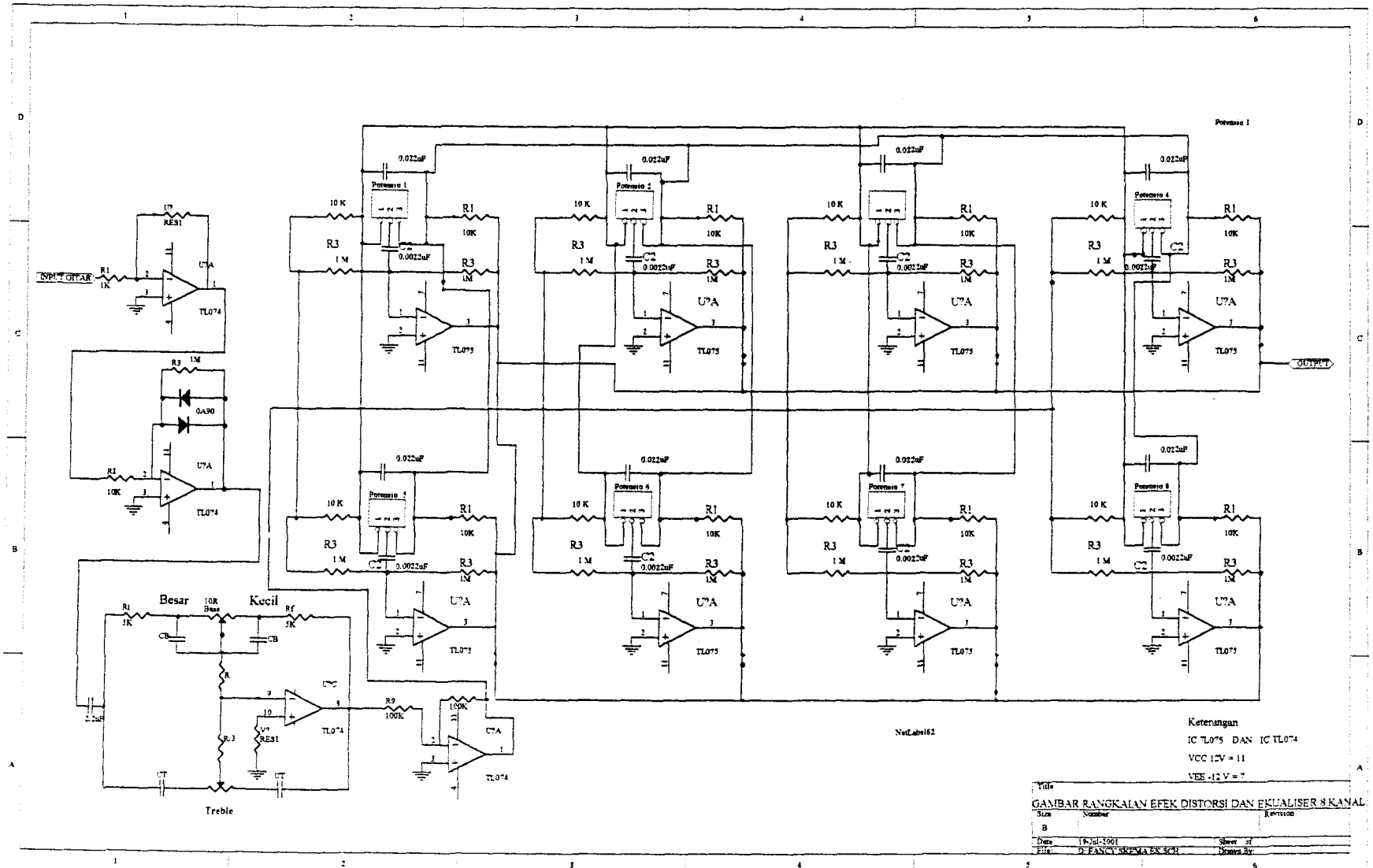


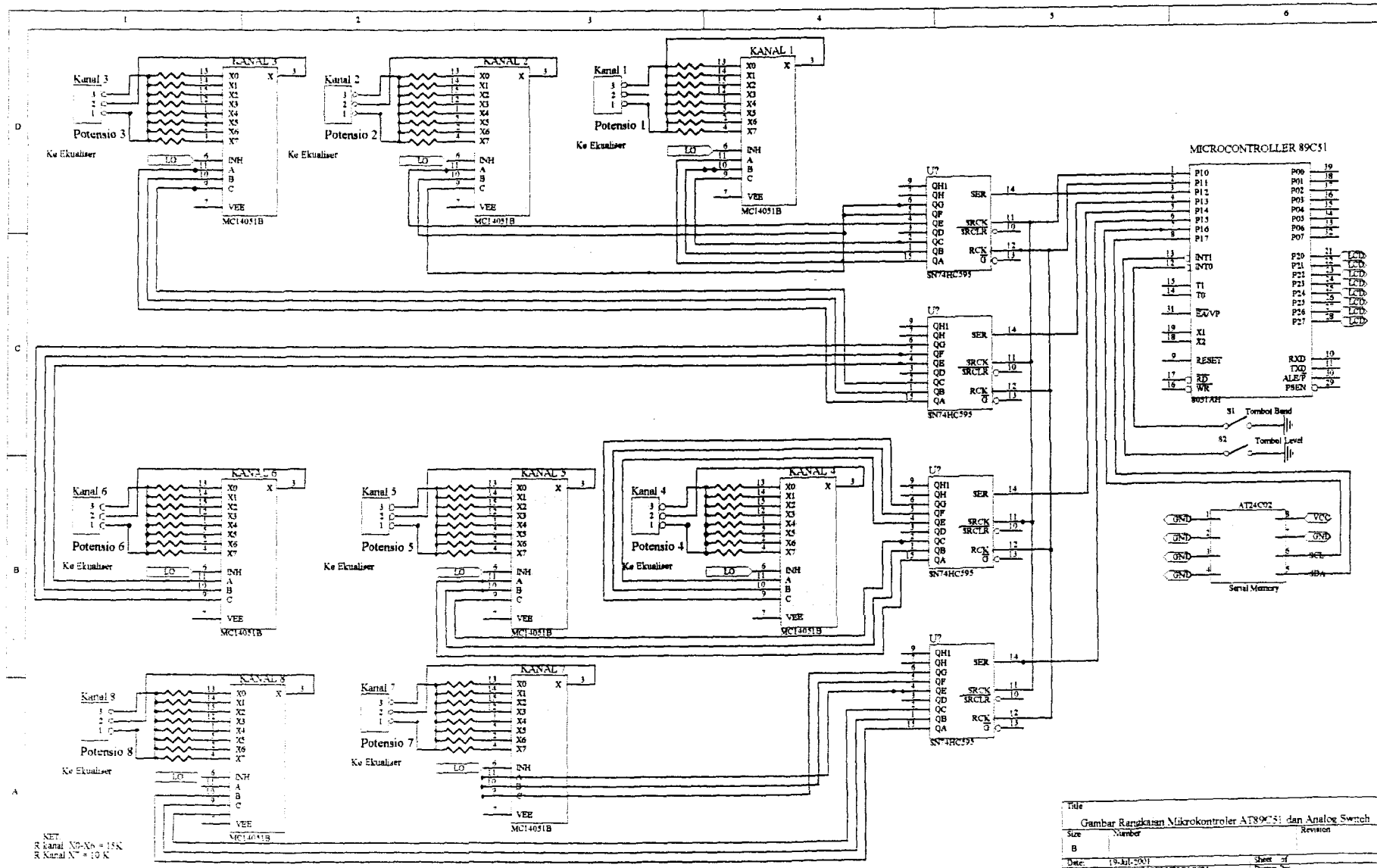
Foto Alat Keseluruhan

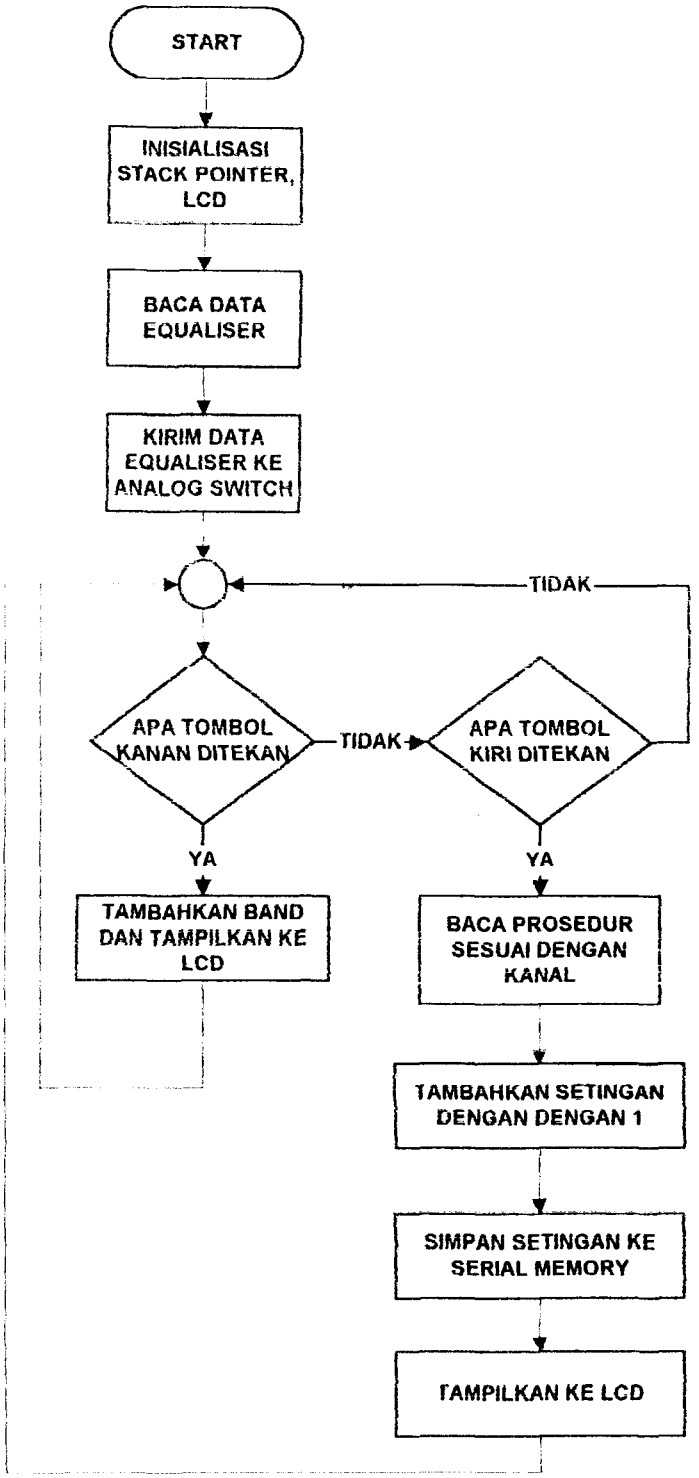


Ket : Frekuensi Input 1 KHz

Tampilan *Oscilloscope* Input dari *Audio Generator* (*Chanel 1*) dan Output alat (*Chanel* 2)


INPUT GITAR
OUTPUT
Potensio 1
Potensio 2
Potensio 3
Potensio 4
Potensio 5
Potensio 6
Potensio 7
Potensio 8
0.022uF
0.0022uF
10 K
1 M
10K
100K
TL074
TL075
0A90
Besar
Kecil
Treble
NetLabel62
Keterangan
IC TL075 DAN IC TL074
VCC 12V = 11
VEE -12 V = 7
GAMBAR RANGKAIAN EFEK DISTORSI DAN EKUALISER 8 KANAL
Size
B
Number
Revision
Date: 19-Jul-2001
Sheet of
File: D:\FANCY\SKEMA EK 8CH.ddb
Drawn By:


KANAL 1
KANAL 2
KANAL 3
KANAL 4
KANAL 5
KANAL 6
KANAL 7
KANAL 8
Kanal 1
Kanal 2
Kanal 3
Kanal 4
Kanal 5
Kanal 6
Kanal 7
Kanal 8
Potensio 1
Potensio 2
Potensio 3
Potensio 4
Potensio 5
Potensio 6
Potensio 7
Potensio 8
Ke Ekualiser
MC14051B
SN74HC595
MICROCONTROLLER 89C51
AT89C51
S1 Tombol Band
S2 Tombol Level
AT24C02
Serial Memory
KET
R Kanal X0-X6 = 15K
R Kanal X7 = 10 K
Gambar Rangkaian Mikrokontroler AT89C51 dan Analog Switch
Size B
Number
Revision
Date: 19-Jul-2003
File: D:\FANCY\SELURUH.SCH
Sheet of
Drawn by:


START
INISIALISASI STACK POINTER, LCD
BACA DATA EQUALISER
KIRIM DATA EQUALISER KE ANALOG SWITCH
TIDAK
APA TOMBOL KANAN DITEKAN
TIDAK
APA TOMBOL KIRI DITEKAN
YA
YA
TAMBAHKAN BAND DAN TAMPILKAN KE LCD
BACA PROSEDUR SESUAI DENGAN KANAL
TAMBAHKAN SETINGAN DENGAN DENGAN 1
SIMPAN SETINGAN KE SERIAL MEMORY
TAMPILKAN KE LCD

PROGRAM *MICROCONTROLLER* AT89C51

```
;p1.0  = sclck
;p1.1  = rclk
;p1.2  = serch12
;p1.3  = serch34
;p1.4  = serch56
;p1.5  = serch78
;p1.6  = clk I2C
;p1.7  = sda I2C
;
;pa    = simulasi lcd        = p2
;pb    = simulasi tombol     = p3.3 & p3.4
;
;
pa          equ   4000h
pb          equ   4001h
pc          equ   4002h
pcw         equ   4003h
cw          equ   82h

ch12        equ   08h
ch34        equ   09h
ch56        equ   0ah
ch78        equ   0bh
band        equ   0ch
free        equ   0dh
data        equ   0eh
memory      equ   0fh


            org   2000h
            ajmp  mulai

            org   2100h
;-------------------------------
;         DELAY 4 mS
;-------------------------------
DELAY4M     MOV   R7,#70
DEL4M       MOV   R6,#250
            DJNZ  R6,$
            DJNZ  R7,DEL4M
            RET
```

```
;-----------------------------
;          START
;-----------------------------
START           SETB P1.7   ;START CONDITION / SCLOCK HIGH
                CLR  P1.6   ;
                SETB P1.6   ;SCLOCK HI TO START CONDITION
                CLR  P1.7   ;SDA HI TO LOW TO START CONDITION
                CLR  P1.6   ;
                RET

;----------------------
;       STOP
;----------------------
STOP            SETB P1.6   ;STOP CONDITION  / SCLOCK HIGH
                SETB P1.7   ;
                RET

;----------------------
;    PROTOCOL WRITE
;----------------------
PROTOCOL MOV    R2,#8
TERUS           RLC  A
                MOV  P1.7,C
                SETB P1.6
                CLR  P1.6
                DJNZ R2,TERUS
                SETB P1.7
                SETB P1.6
                MOV  C,P1.7             ;"ACK" SAVED IN CARRY
                CLR  P1.6
                CLR  P1.7
                RET

;----------------------
;       WRITE
;----------------------
WRITE           ACALL       START
          MOV       A,#0A0H           ;CODE WRITE MEMORY
             ACALL       PROTOCOL
          MOV       A,MEMORY
          ACALL     PROTOCOL
          MOV       A,DATA
          ACALL     PROTOCOL
             ACALL       STOP
             MOV  R7,#250             ;DELAY WRITE TO SERIAL MEMORY
             DJNZ R7,$
```

```
            RET
;---------------------
;       READ
;---------------------
READ        ACALL       START
            MOV  A,#0A0H      ;CODE WRITE UTK MENENTUKAN ALAMAT
            ACALL       PROTOCOL
            MOV  A,MEMORY
            ACALL       PROTOCOL
            ACALL       START
            MOV  A,#0A1H      ;CODE BACA MEMORY
            ACALL       PROTOCOL
            MOV  R2,#8
            SETB P1.7         ;SDA --> INPUT
BACA        SETB P1.6
            MOV  C,P1.7
            RLC  A
            CLR  P1.6
            DJNZ R2,BACA
            SETB P1.7         ;CEK "NO ACK"
            SETB P1.6
            CLR  P1.6
            CLR  P1.7
            ACALL       STOP
            MOV  DATA,A
            RET

;-----------------------------
;      DELAY ( 2 SECON )
;-----------------------------
DELAY2          MOV  R5,#3
DEL5        MOV  R6,#250
DEL6        MOV  R7,#250
            DJNZ R7,$
            DJNZ R6,DEL6
            DJNZ R5,DEL5
            RET


;-----------------------------
;   ENABLE PULSE for LCD
;-----------------------------
ENABLE       MOV    DPTR,#PA
            ANL    A,#0FH
            MOVX   @DPTR,A
            ORL    A,#20H
```

```
            MOVX   @DPTR,A
            ANL    A,#0FH
            MOVX   @DPTR,A
            ACALL  DELAY4M
            RET

;---------------------------
;       CONTROL LCD
;---------------------------
LCDCONTROL    MOV    FREE,A
            SWAP   A
            ACALL  ENABLE
            MOV    A,FREE
            ACALL  ENABLE
            RET

;---------------------------
;   INISILISASI LCD 4 BIT
;---------------------------
INITLCD4BIT   MOV    DPTR,#PA
            MOV    R5,#3

WAIT        MOV    A,#3H
            MOVX   @DPTR,A
            ORL    A,#20H
            MOVX   @DPTR,A
            ANL    A,#0FH
            MOVX   @DPTR,A
            ACALL  DELAY4M
            DJNZ   R5,WAIT

WAITFUNCT     MOV    A,#2H        ;FUNCTION SET
            MOVX   @DPTR,A
            ORL    A,#20H
            MOVX   @DPTR,A
            ANL    A,#0FH
            MOVX   @DPTR,A
            ACALL  DELAY4M

            MOV    A,#2FH       ;FUNCTIONSET
            ACALL  LCDCONTROL
            MOV    A,#0CH       ;DISPLAY ON
            ACALL  LCDCONTROL
            MOV    A,#01H       ;DISPLAY CLEAR
            ACALL  LCDCONTROL
            MOV    A,#06H       ;ENTRY
```

```
                ACALL   LCDCONTROL
                RET

;---------------------------
;       CETAK TO LCD
;---------------------------
CETAK           ANL     A,#0FH
                ORL     A,#10H
                MOVX    @DPTR,A
                ORL     A,#20H
                MOVX    @DPTR,A
                ANL     A,#1FH
                MOVX    @DPTR,A
                MOV     R7,#50
                DJNZ    R7,$
                RET

;---------------------------
;       DISPLAY LCD
;---------------------------
LCD             MOV     DPTR,#PA
                MOV     FREE,A
                SWAP    A
                ACALL   CETAK
                MOV     A,FREE
                ACALL   CETAK
                RET

;---------------------------
;           delay
;---------------------------
delay           mov     r7,#250
dela            mov     r6,#250
                djnz    r6,$
                djnz    r7,dela
                ret

;---------------------------
;  loading data equaliser
;---------------------------
loading                 mov     r6,#4
                mov     memory,#10h             ;offset address 10h I2C
                mov     r0,#08h
nextload        acall   read
                inc     memory
                mov     @r0,data
```

```
                inc     r0
                djnz    r6,nextload
                ret

;----------------------------
; value of set saved into I2C
;----------------------------
saveto_i2c      mov     r0,#08h
                mov     r6,#4
                mov     memory,#10h
nextsave        mov     data,@r0
                acall   write
                inc     r0
                inc     memory
                djnz    r6,nextsave
                ret

;----------------------------
;       serial output
;----------------------------
serial_out      mov     r7,#8
nextserial      mov     a,ch12
                rlc     a
                mov     p1.2,c
                mov     a,ch12
                rl      a
                mov     ch12,a

                mov     a,ch34
                rlc     a
                mov     p1.3,c
                mov     a,ch34
                rl      a
                mov     ch34,a

                mov     a,ch56
                rlc     a
                mov     p1.4,c
                mov     a,ch56
                rl      a
                mov     ch56,a

                mov     a,ch78
                rlc     a
                mov     p1.5,c
                mov     a,ch78
```

```
                rl      a
                mov     ch78,a
                clr     p1.0            ;pulse serclock
                setb    p1.0
                djnz    r7,nextserial
                clr     p1.1            ;lacth enable
                setb    p1.1
                ret

;---------------------------
;       set equliser
;---------------------------
set             mov     a,band
                jz      back
                mov     dptr,#jumptable
                mov     c,acc.0
                mov     psw.1,c
                clr     c
                dec     a
                rrc     a
                mov     b,#2
                mul     ab
                jmp     @a+dptr
back            ret
jumptable       ajmp    band_ch12
                ajmp    band_ch34
                ajmp    band_ch56
                ajmp    band_ch78

;---------------------------- Band 1 & 2 ----------------------------------
band_ch12       mov     a,ch12
                jnb     psw.1,ch_even12
                inc     ch12
                jnb     acc.3,pass_ch12         ;cek apakah ch1 = 7 ?
                anl     ch12,#0f0h
                ajmp    back

ch_even12       swap    a
                inc     a
                swap    a
                mov     ch12,a
                jnb     acc.7,pass_ch12         ;cek apakah ch2 = 7 ?
                anl     ch12,#0fh
pass_ch12       ajmp    back

;---------------------------- Band 3 & 4 ----------------------------------
```

```
band_ch34   mov   a,ch34
            jnb   psw.1,ch_even34
            inc   ch34
            jnb   acc.3,pass_ch34          ;cek apakah ch3 = 7 ?
            anl   ch34,#0f0h
            ajmp  back

ch_even34   swap  a
            inc   a
            swap  a
            mov   ch34,a
            jnb   acc.7,pass_ch34          ;cek apakah ch4 = 7 ?
            anl   ch34,#0fh
pass_ch34   ajmp  back
;---------------------------- Band 5 & 6 ----------------------------------
band_ch56   mov   a,ch56
            jnb   psw.1,ch_even56
            inc   ch56
            jnb   acc.3,pass_ch56          ;cek apakah ch1 = 7 ?
            anl   ch56,#0f0h
            ajmp  back

ch_even56   swap  a
            inc   a
            swap  a
            mov   ch56,a
            jnb   acc.7,pass_ch56
            anl   ch56,#0fh
pass_ch56   ajmp  back
;---------------------------- Band 7 & 8 ----------------------------------
band_ch78   mov   a,ch78
            jnb   psw.1,ch_even78
            inc   ch78
            jnb   acc.3,pass_ch78          ;cek apakah ch1 = 7 ?
            anl   ch78,#0f0h
            ajmp  back

ch_even78   swap  a
            inc   a
            swap  a
            mov   ch78,a
            jnb   acc.7,pass_ch78
            anl   ch78,#0fh
pass_ch78   ajmp  back
```

```
;----------------------------
;   select band equaliser
;----------------------------
select_band  inc     band
             mov     a,band
             cjne    a,#9,sel_bandpres
             mov     band,#0
sel_bandpres   jnb   p1.6,$              ;wait until not keypressed
             ret

;----------------------------
;       display lcd
;----------------------------
display              mov   a,#80h
             acall   lcdcontrol          ;baris 1
             mov     a,band
             mov     b,#16
             mul     ab

             mov     dptr,#table_kata
             add     a,dpl
             mov     dpl,a
             mov     a,#0
             addc    a,dph
             mov     dph,a
             mov     r2,#16
nextchar     mov     a,#0
             movc    a,@a+dptr
             push    dph
             push    dpl
             acall   lcd
             pop     dpl
             pop     dph
             inc     dptr
             djnz    r2,nextchar

             mov     a,#0c0h                 ;line 2
             acall   lcdcontrol
             mov     r2,#7
dispblank    mov     a,#20h
             acall   lcd                 ;disp 7th times
             djnz    r2,dispblank

             mov     a,band
             jnz     nilai_set       ;if no band selection then
             mov     r2,#10                  ;lcd line 2 blank
```

```
printblank      mov   a,#20h                    ;cetak space
                acall lcd
                djnz  r2,printblank
                ajmp  escdisplay

nilai_set       ;mov  c,acc.0
                ;mov  psw.1,c
                ;clr  c
                ;dec  a
                ;rrc  a
                ;mov  b,#2
                ;mul  ab
                ;mov  dptr,#tabledisp_ch
                ;jmp  @a+dptr
escdisplay      ret

table_kata      db    'No Band Selected'
                db    '   Band 1   '
                db    '   Band 2   '
                db    '   Band 3   '
                db    '   Band 4   '
                db    '   Band 5   '
                db    '   Band 6   '
                db    '   Band 7   '
                db    '   Band 8   '
tabledisp_ch    ajmp  loadch12
                ajmp  loadch34
                ajmp  loadch56
                ajmp  loadch78

;------------------------ load value ch12 to lcd ----------------------------------------
loadch12        jnb   psw.1,evench12            ;ch1 or ch2 ?
                mov   a,ch12
                anl   a,#0fh
                orl   a,#30h                    ;disp number in ASCII

                acall lcd
                ajmp  tabledisp_ch
evench12        mov   a,ch12
                swap  a
                anl   a,#0fh
                orl   a,#30h
                acall lcd
                ajmp  tabledisp_ch
;------------------------ load value ch34 to lcd ----------------------------------------
loadch34        jnb   psw.1,evench34            ;ch3 or ch4 ?
```

```
                mov   a,ch34
                anl   a,#0fh
                orl   a,#30h                    ;disp number in ASCII

                acall lcd
                ajmp  tabledisp_ch
evench34        mov   a,ch34
                swap  a
                anl   a,#0fh
                orl   a,#30h
                acall lcd
                ajmp  tabledisp_ch
;------------------------ load value ch56 to lcd ----------------------------------------
loadch56        jnb   psw.1,evench56            ;ch5 or ch6 ?
                mov   a,ch56
                anl   a,#0fh
                orl   a,#30h                    ;disp number in ASCII

                acall lcd
                ajmp  tabledisp_ch
evench56        mov   a,ch56
                swap  a
                anl   a,#0fh
                orl   a,#30h
                acall lcd
                ajmp  tabledisp_ch
;------------------------ load value ch78 to lcd ----------------------------------------
loadch78        jnb   psw.1,evench78            ;ch7 or ch8 ?
                mov   a,ch78
                anl   a,#0fh
                orl   a,#30h                    ;disp number in ASCII

                acall lcd
                ajmp  tabledisp_ch
evench78        mov   a,ch78
                swap  a
                anl   a,#0fh
                orl   a,#30h
                acall lcd
                ajmp  tabledisp_ch

;---------------------------
;       main program
;---------------------------
mulai           mov   sp,#40h
                acall delay
```

```
                mov   dptr,#pcw
                mov   a,#cw
                movx  @dptr,a
                acall initlcd4bit
                acall loading
                acall serial_out
                mov   band,#1
                acall display
                setb  p1.6
                setb  p1.7

ulang           mov   dptr,#pb
                movx  a,@dptr
                jb    acc.0,cek_set
                ;jb   p1.6,cek_set        ;tombol band ditekan ?
                acall select_band
                acall display
                ajmp  ulang

cek_set         jb    acc.1,ulang
                ;jb   p1.7,pas            ;tombol set ditekan ?
                acall set
                acall serial_out
                acall display
                acall saveto_i2c
pas             ajmp  ulang
```

ıtures

- ite Protect Pin for Hardware Data Protection
  - Utilizes Different Array Protection Compared to the AT24C02/04/08
- w-voltage and Standard-voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- ernally Organized 256 x 8 (2K), 512 x 8 (4K) or 1024 x 8 (8K)
- vire Serial Interface
- hmitt Trigger, Filtered Inputs for Noise Supperssion
- lirectional Data Transfer Protocol
-) kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Clock Rate
- yte Page (2K), 16-byte Page (4K, 8K) Write Modes
- tial Page Writes are Allowed
- f-timed Write Cycle (10 ms max)
- gh Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V
- tomotive Grade and Extended Temperature Devices Available
- ead JEDEC SOIC, 8-pin PDIP, and 8-lead TSSOP Packages

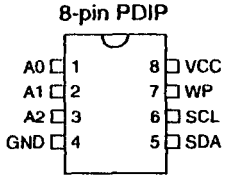
scription

AT24C02A/04A/08A provides 2048/4096/8192 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 256/512/1024 words bits each. The device is optimized for use in many industrial and commercial ications where low power and low voltage operation are essential. The 4C02A/04A/08A is available in space saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP (AT24C02A/04A) packages and is accessed via a 2-wire serial face. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V 5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

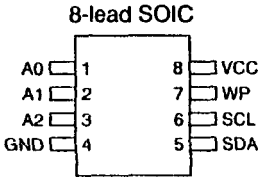
Configurations

Name	Function
- A2	Address Inputs
\	Serial Data
.	Serial Clock Input
	Write Protect
	No Connect

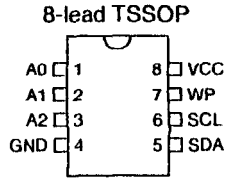
8-pin PDIP



8-lead SOIC



8-lead TSSOP



2-wire Serial EEPROM

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

AT24C02A
AT24C04A
AT24C08A

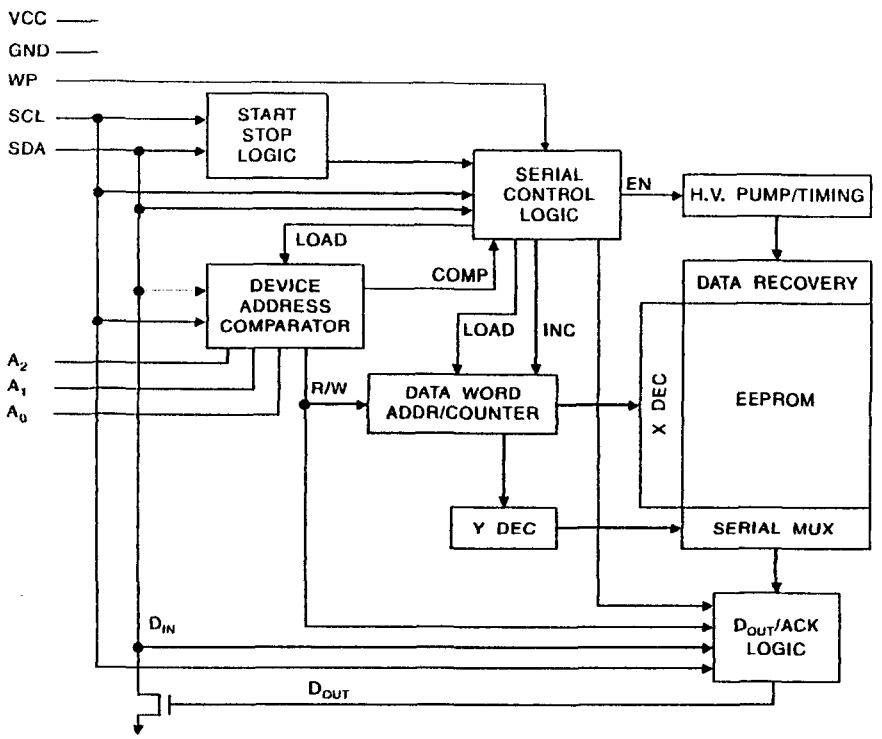
Rev. 0976C–04/01

)solute Maximum Ratings*

)erating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
ltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.25V
: Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ock Diagram



n Description

RIAL CLOCK (SCL): The SCL input is used to positive ge clock data into each EEPROM device and negative ge clock data out of each device.

RIAL DATA (SDA): The SDA pin is bidirectional for ial data transfer. This pin is open-drain driven and may wire-ORed with any number of other open-drain or open ector devices.

VICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 A0 pins are device address inputs that are hard wired the AT24C02A. As many as eight 2K devices may be dressed on a single bus system (device addressing is cussed in detail under the Device Addressing section).

The AT24C04A uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

WRITE PROTECT (WP): The AT24C02A/04A/08A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect

Features

- **Compatible with MCS-51™ Products**
- **4 Kbytes of In-System Reprogrammable Flash Memory**
  Endurance: 1,000 Write/Erase Cycles
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

8-Bit Microcontroller with 4 Kbytes Flash

AT89C51

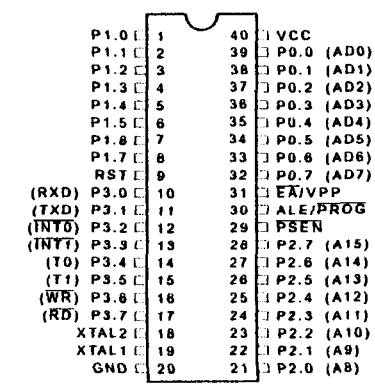
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

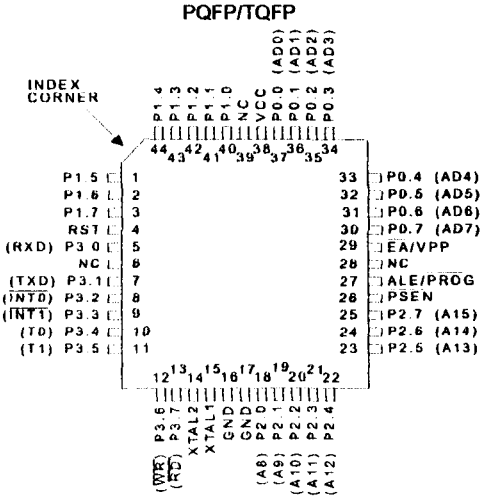
(continued)

Pin Configurations

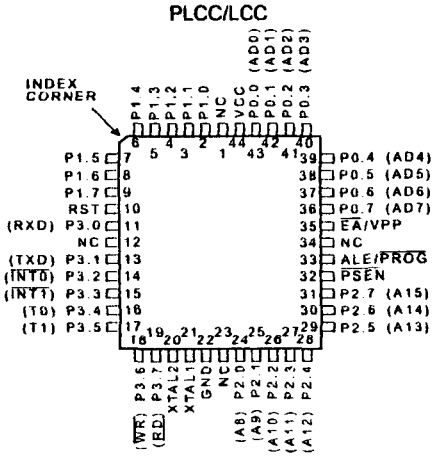
PDIP/Cerdip



PQFP/TQFP

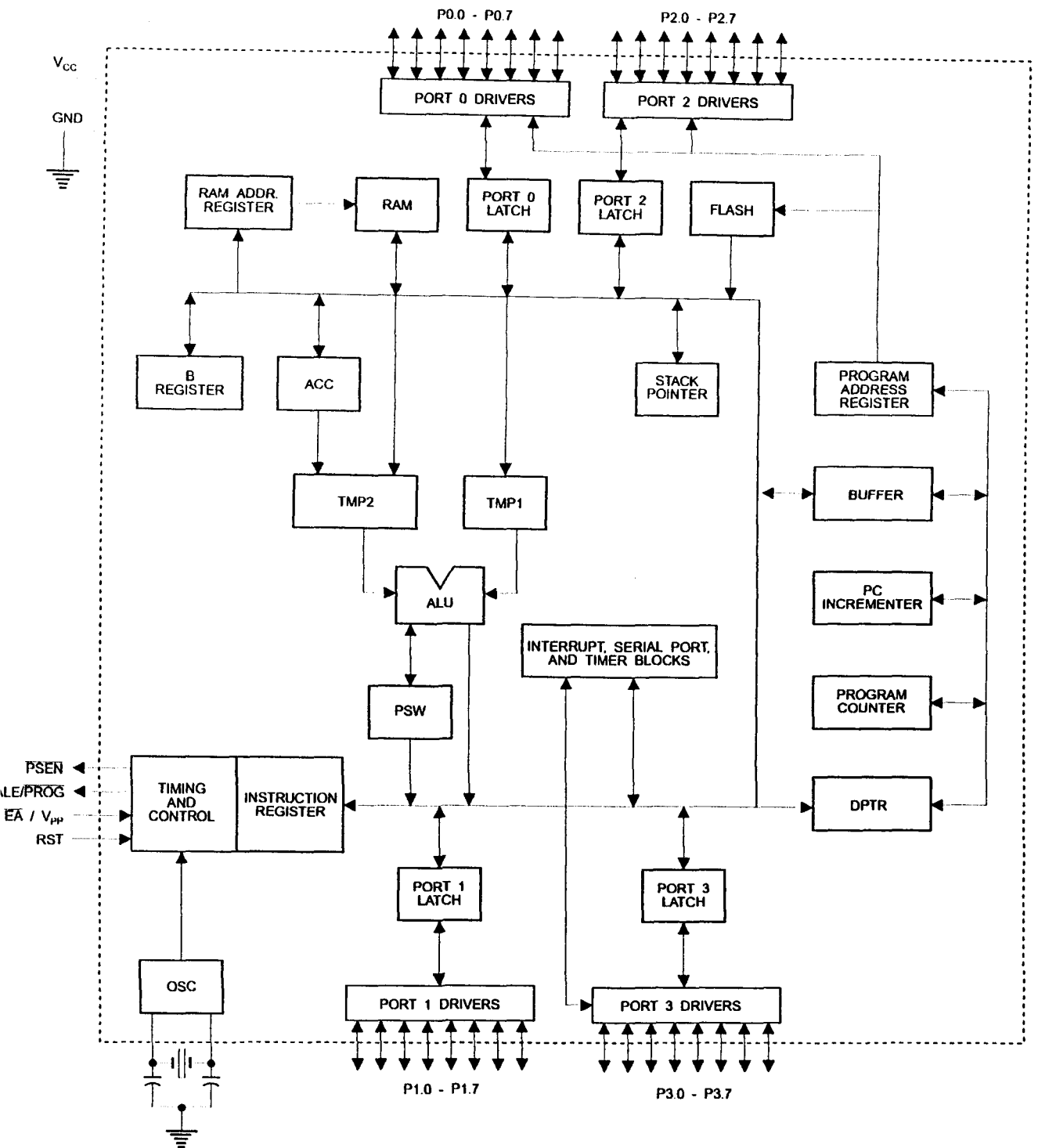


PLCC/LCC



0265E

Block Diagram



ıescription (Continued)

ıe AT89C51 provides the following standard features: 4 bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit ner/counters, a five vector two-level interrupt architecre, a full duplex serial port, on-chip oscillator and clock rcuitry. In addition, the AT89C51 is designed with static gic for operation down to zero frequency and supports vo software selectable power saving modes. The Idle lode stops the CPU while allowing the RAM, timer/countrs, serial port and interrupt system to continue functionıg. The Power Down Mode saves the RAM contents but eezes the oscillator disabling all other chip functions until ıe next hardware reset.

?in Description

cc

ıupply voltage.

;ND

;round.

'ort 0

?ort 0 is an 8-bit open drain bidirectional I/O port. As an ıutput port each pin can sink eight TTL inputs. When 1s ıre written to port 0 pins, the pins can be used as high-imıedance inputs.

?ort 0 may also be configured to be the multiplexed lowırder address/data bus during accesses to external proıram and data memory. In this mode P0 has internal pulups.

?ort 0 also receives the code bytes during Flash programning, and outputs the code bytes during program verificaion. External pullups are required during program verificaion.

?ort 1

?ort 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by he internal pullups and can be used as inputs. As inputs, ?ort 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

?ort 1 also receives the low-order address bytes during Flash programming and program verification.

?ort 2

?ort 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by he internal pullups and can be used as inputs. As inputs, ?ort 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

?ort 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (extenal interrupt 0)
P3.3	$\overline{INT1}$ (extenal interrupt 1)
P3.4	T0 (timer 0 extenal input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (extenal data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcrontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

(continued)

Pin Description (Continued)

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

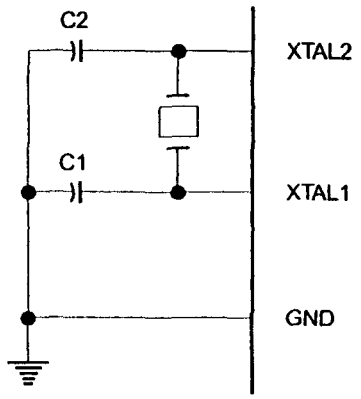
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

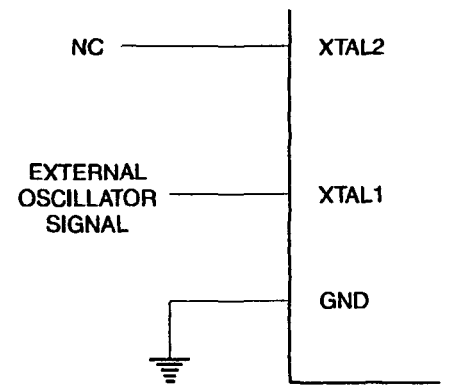
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC4051
MC54/74HC4052
MC54/74HC4053

Advance Information

Analog Multiplexers/ Demultiplexers

High-Performance Silicon-Gate CMOS

The MC54/74HC4051, MC54/74HC4052, and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051, HC4052, and HC4053 are identical in pinout to the metal-gate MC14051B, MC14052B, and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal-gate CMOS analog switches.

For multiplexers/demultiplexers with channel select latches, see HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4051—184 FETs or 46 Equivalent Gates
  HC4052—168 FETs or 42 Equivalent Gates
  HC4053—156 FETs or 39 Equivalent Gates

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-06

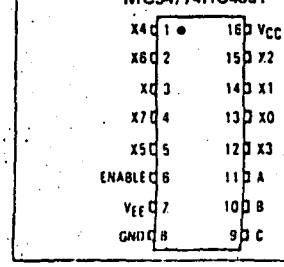
DW SUFFIX
SOIC
CASE 751G-01

ORDERING INFORMATION

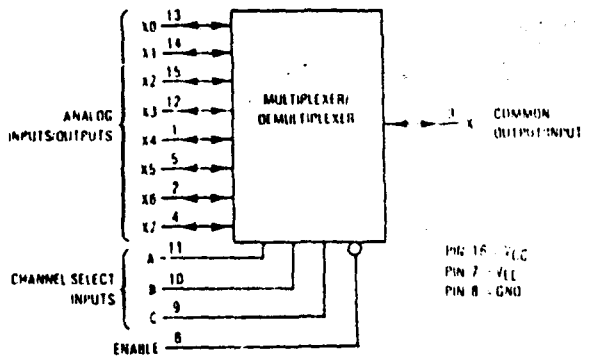
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT
MC54/74HC4051



LOGIC DIAGRAM
MC54/74HC4051
Single-Pole, 8-Position Plus Common Off



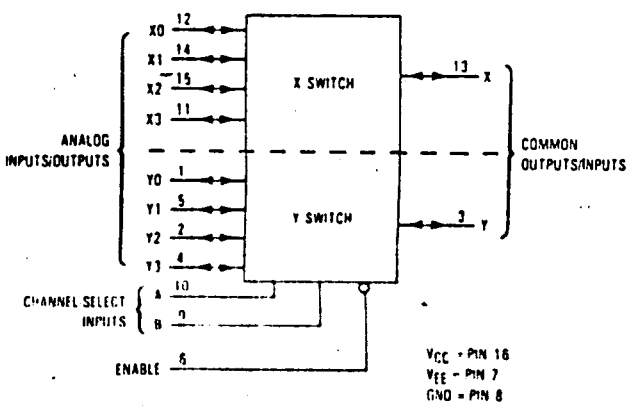
FUNCTION TABLE
MC54/74HC4051

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	None

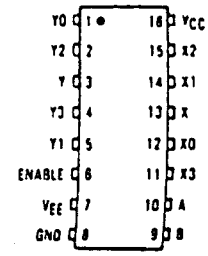
X = don't care

MC54/74HC4052
Double-Pole, 4-Position
Plus Common Off

LOGIC DIAGRAM



PIN ASSIGNMENT



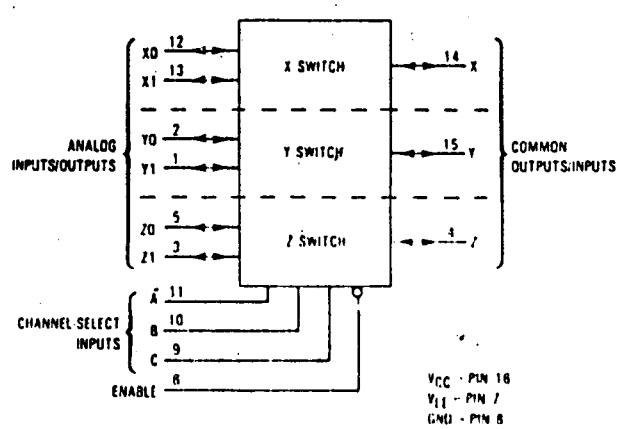
FUNCTION TABLE

Control Inputs			
Enable	Select		ON Channels
	B	A	
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 Y
H	X	X	None

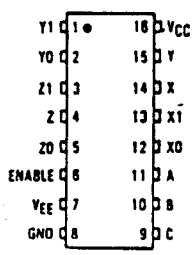
X = Don't Care

MC54/74HC4053
Triple Single-Pole, Double-Position
Plus Common Off

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs						
Enable	Select			ON Channels		
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

X = Don't Care

NOTE: This device allows independent control of each switch. Channel Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	−0.5 to +7.0 −0.5 to 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	−7.0 to +0.5	V
V_{IS}	Analog Input Voltage	V_{EE} −0.5 to V_{CC} +0.5	V
V_{in}	Digital Input Voltage (Ref. to GND)	−1.5 to V_{CC} +1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P_D	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	 750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated. See Applications Information

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Power Dissipation Temperature Derating:
Plastic "N" Package: −10 mW/°C from 65° to 85°C
Ceramic "J" Package: −10 mW/°C from 100° to 125°C
SOIC "D" Package: −7 mW/°C from 65° to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})		2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		−6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		—	1.2	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time, (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = −6.0 V	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enable = V_{CC} or GND V_{IS} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = −6.0	 6.0 6.0	 2 8	 20 80	 40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC}	V_{EE}	Guaranteed Limit			Unit
					25°C to −55°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ to V_{EE} $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 −4.5 −6.0	190 120 100	240 150 125	280 170 140	Ω
		$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 −4.5 −6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = 1/2\ (V_{CC} - V_{EE})$ $I_S \le 2.0$ mA	4.5 4.5 6.0	0.0 −4.5 −6.0	30 12 10	35 15 12	40 18 14	Ω
I_{off}	Maximum Off Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} - V_{EE}$ Switch Off (Figure 3)	6.0	−6.0	0.1	0.5	1.0	μA
	Maximum Off Channel Leakage Current, Common Channel HC4051	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} - V_{EE}$ Switch Off (Figure 4)	6.0	−6.0	0.2	2.0	4.0	
	HC4052		6.0	−6.0	0.1	1.0	2.0	
	HC4053		6.0	−6.0	0.1	1.0	2.0	
I_{on}	Maximum On-Channel Leakage Current, Channel to Channel HC4051	$V_{in} = V_{IL}$ or V_{IH} Switch to Switch = $V_{CC} - V_{EE}$ (Figure 5)	6.0	−6.0	0.2	2.0	4.0	μA
	HC4052		6.0	−6.0	0.1	1.0	2.0	
	HC4053		6.0	−6.0	0.1	1.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH} t_{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 4.5 6.0	290 58 49	364 73 62	430 86 73	ns
t_{PZL} t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns
C_{in}	Maximum Input Capacitance, Channel-Select or Enable Inputs	–	10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O (All Switches Off)	–	35	35	35	pF
	Common O/I: HC4051	–	130	130	130	
	HC4052		80	80	80	
	HC4053		50	50	50	
	Feedthrough	–	1.0	1.0	1.0	

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) (Figure 13) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V 45 (HC4051) 80 (HC4052) 45 (HC4053)	pF

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Condition	V_{CC} V	V_{EE} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads −3 dB R_L = 50 Ω, C_L = 10 pF			51 52 53	MHz
			2.25	−2.25	80 95 120	
			4.50	−4.50	80 95 120	
			6.00	−6.00	80 95 120	
—	Off Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25	−2.25	−50	dB
			4.50	−4.50	−50	
			6.00	−6.00	−50	
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25	−2.25	−40	
			4.50	−4.50	−40	
			6.00	−6.00	−40	
—	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V_{in} ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A Enable = GND R_L = 600 Ω, C_L = 50 pF	2.25	−2.25	25	mVpp
			4.50	−4.50	105	
			6.00	−6.00	135	
		R_L = 10 kΩ, C_L = 10 pF	2.25	−2.25	35	
			4.50	−4.50	145	
			6.00	−6.00	190	
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051)	f_{in} = Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25	−2.25	−50	dB
			4.50	−4.50	−50	
			6.00	−6.00	−50	
		f_{in} = 1 MHz, R_L = 50 Ω, C_L = 10 pF	2.25	−2.25	−60	
			4.50	−4.50	−60	
			6.00	−6.00	−60	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 Vpp sine wave	2.25	−2.25	0.10	
		V_{IS} = 8.0 Vpp sine wave	4.50	−4.50	0.08	
		V_{IS} = 11.0 Vpp sine wave	6.00	−6.00	0.05	

* Units not tested. Determined by design and verified by qualification.

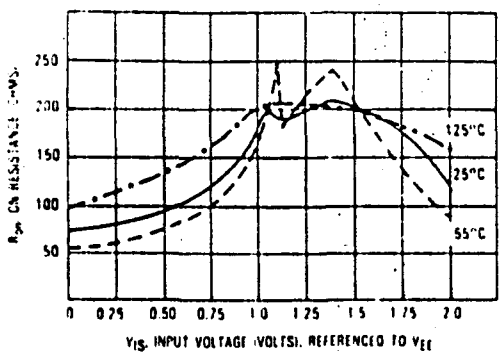


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

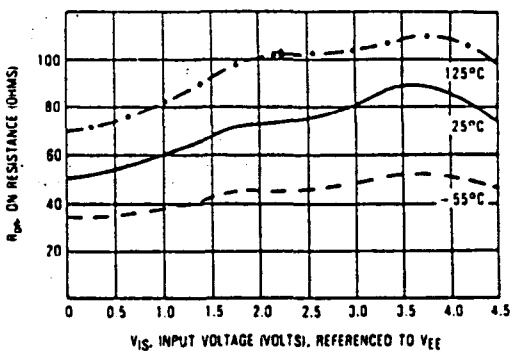


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

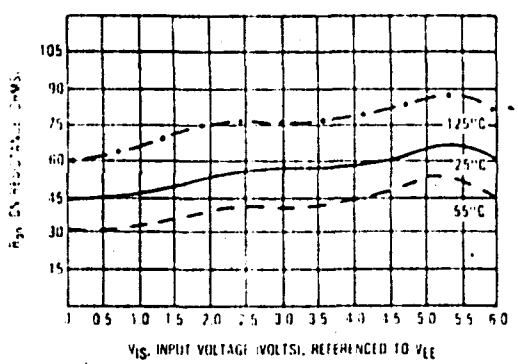


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

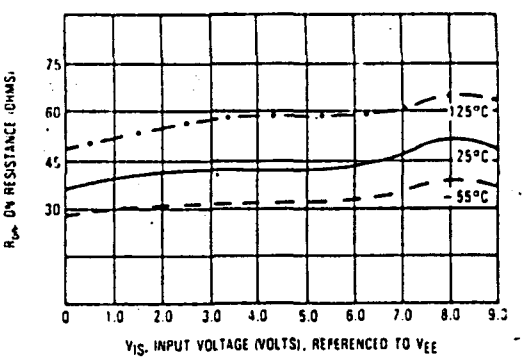


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

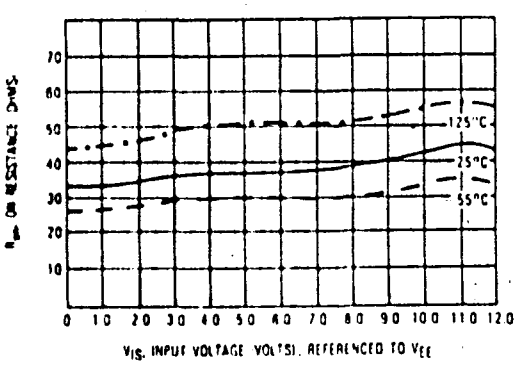


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

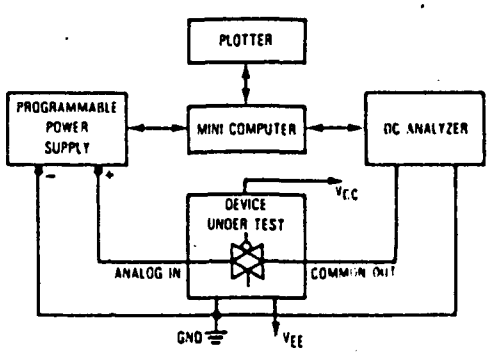


Figure 2. On Resistance Test Set-Up

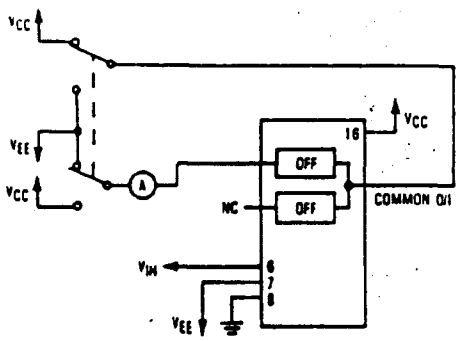


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

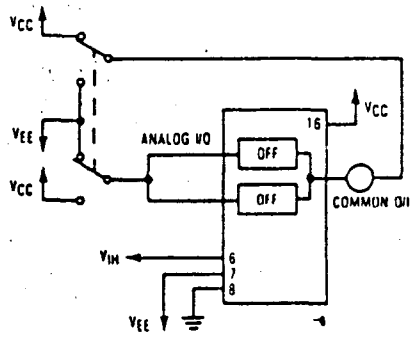


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

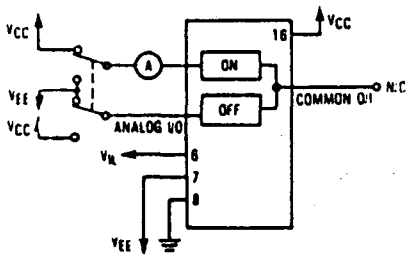
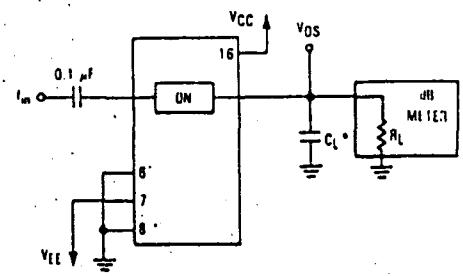
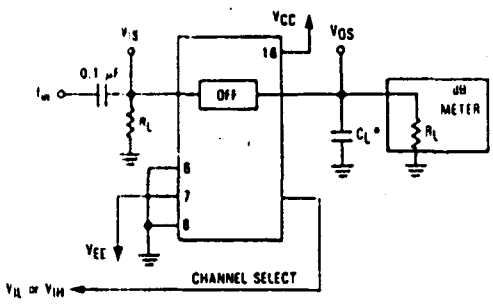


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



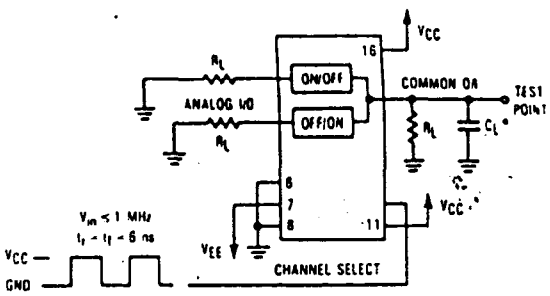
*Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

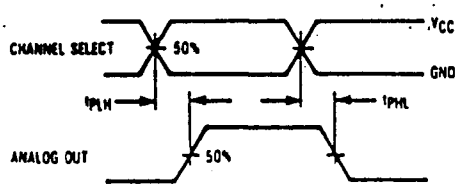
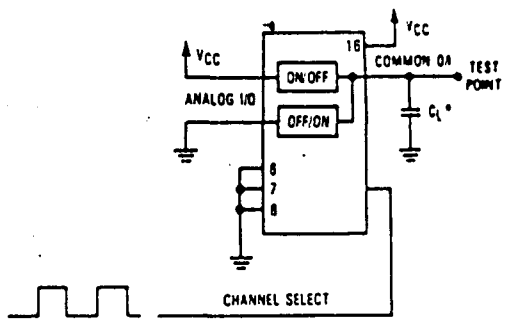


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

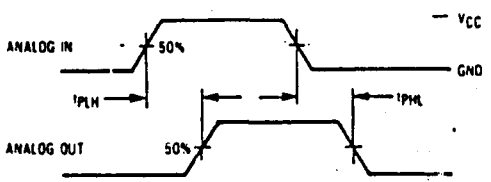
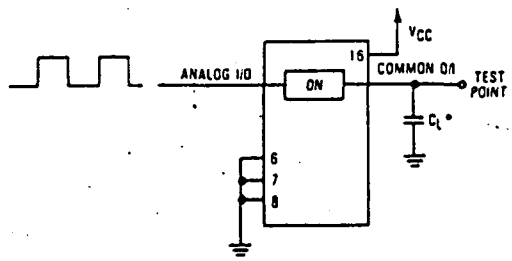


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

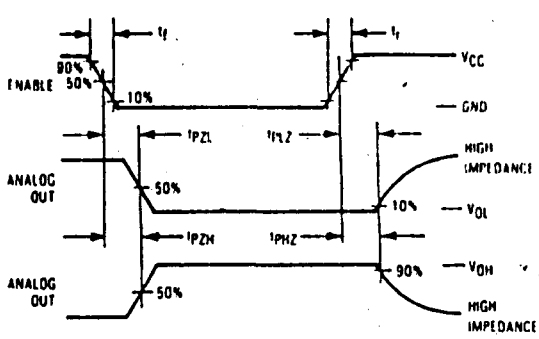


Figure 11a. Propagation Delays, Enable to Analog Out

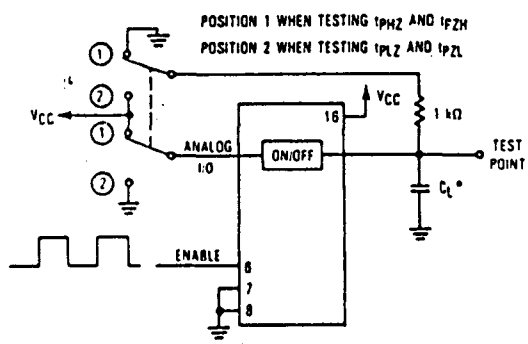
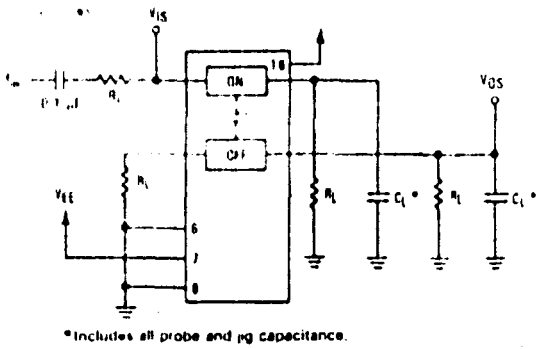


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

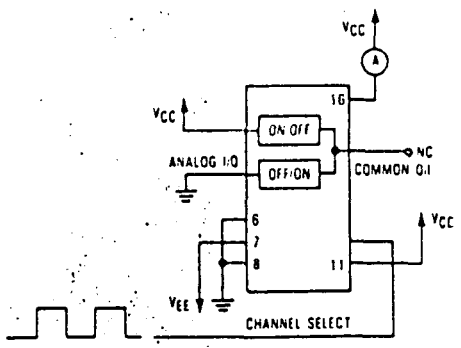
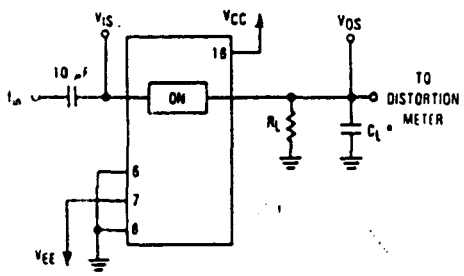


Figure 13. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

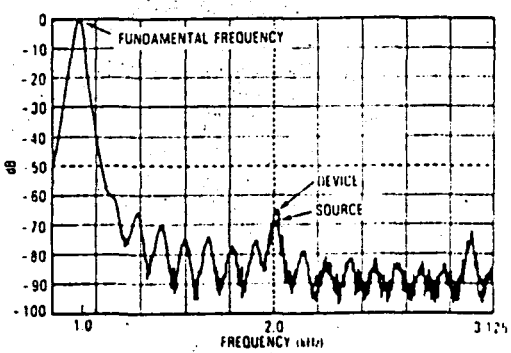


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5 V = logic high
GND = 0 V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked-up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts
V_{EE} – GND = 0 to – 6 volts
V_{CC} – V_{EE} = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

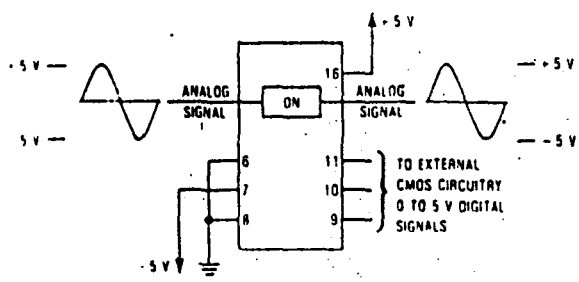


Figure 15. Application Example

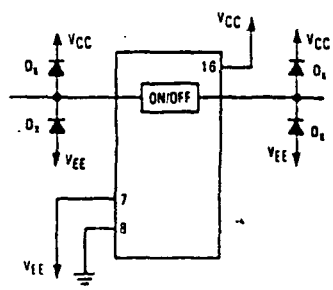
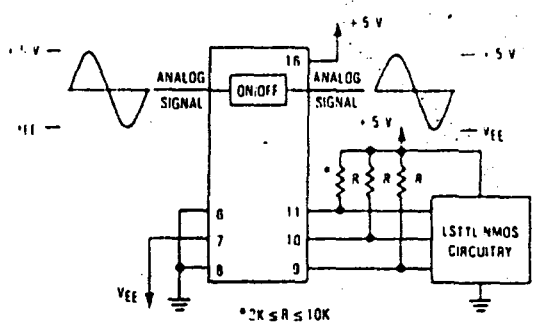
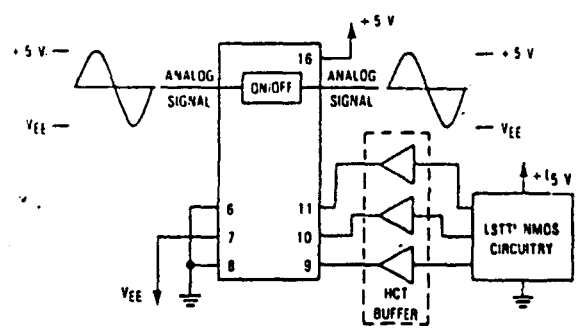


Figure 16. External Germanium or Schottky Clipping Diodes



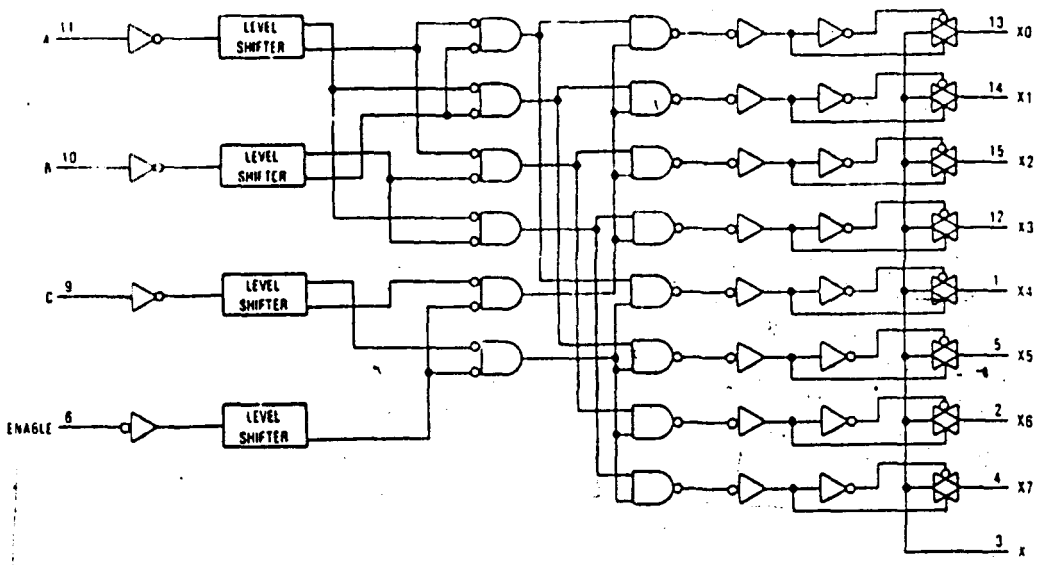
a. Using Pull-Up Resistors



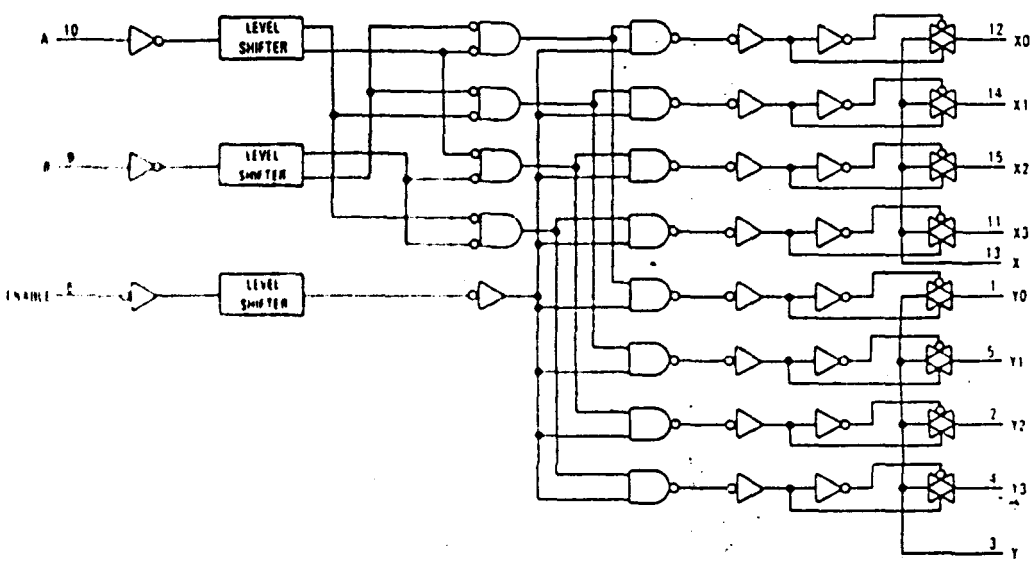
b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

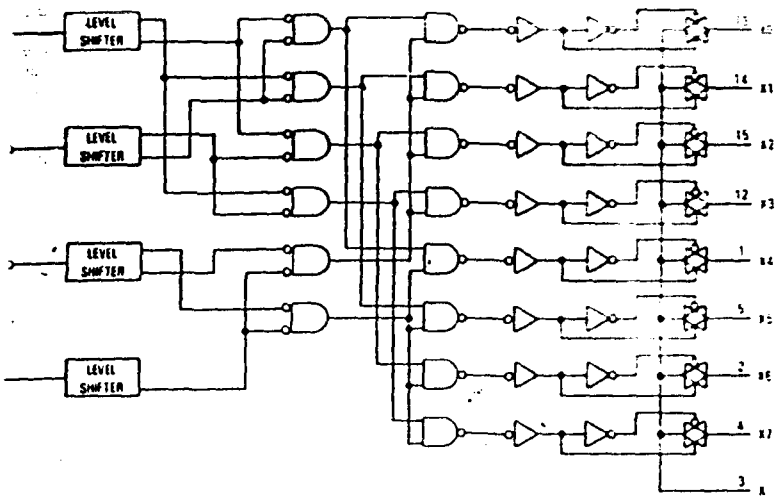
FUNCTION DIAGRAM, HC4051



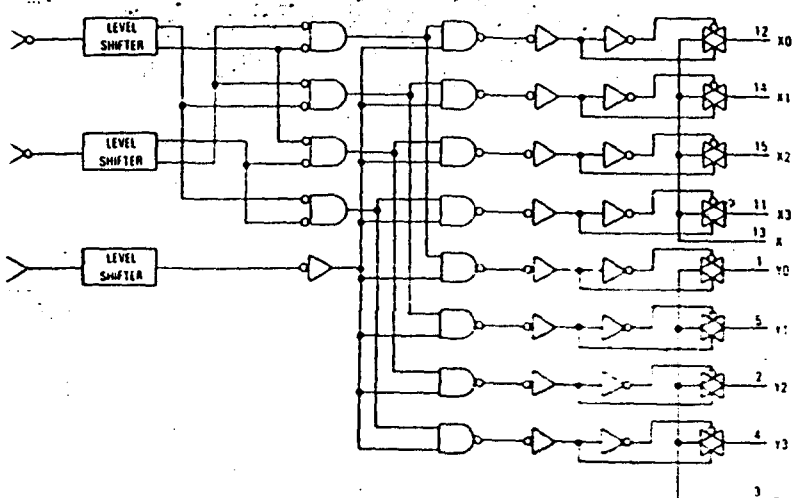
FUNCTION DIAGRAM, HC4052



FUNCTION DIAGRAM, HC4051

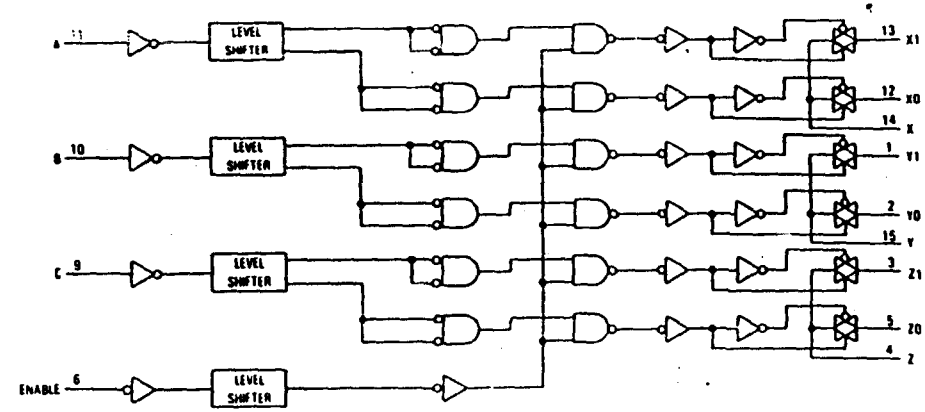


FUNCTION DIAGRAM, HC4052



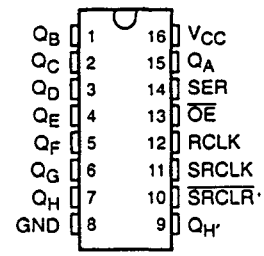
MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

FUNCTION DIAGRAM, HC4053

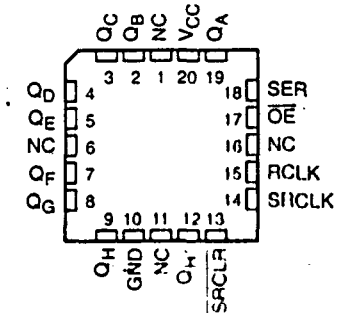


- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **8-Bit Serial-In, Parallel-Out Shift**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT595 . . . J OR W PACKAGE
SN74AHCT595 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT595 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

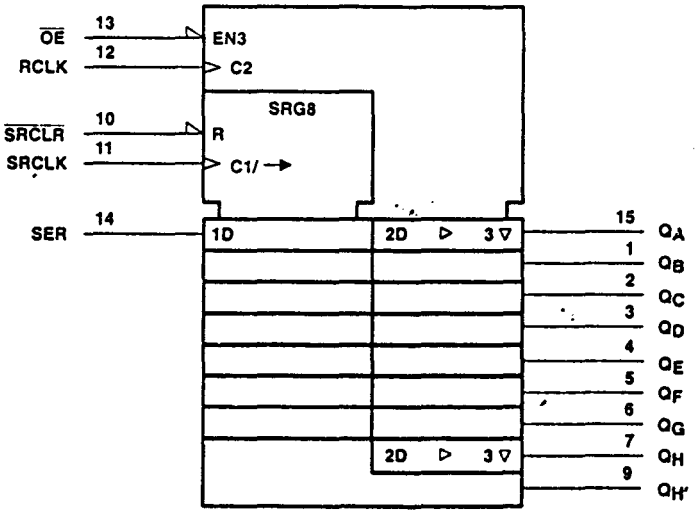
Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The SN54AHCT595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT595 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

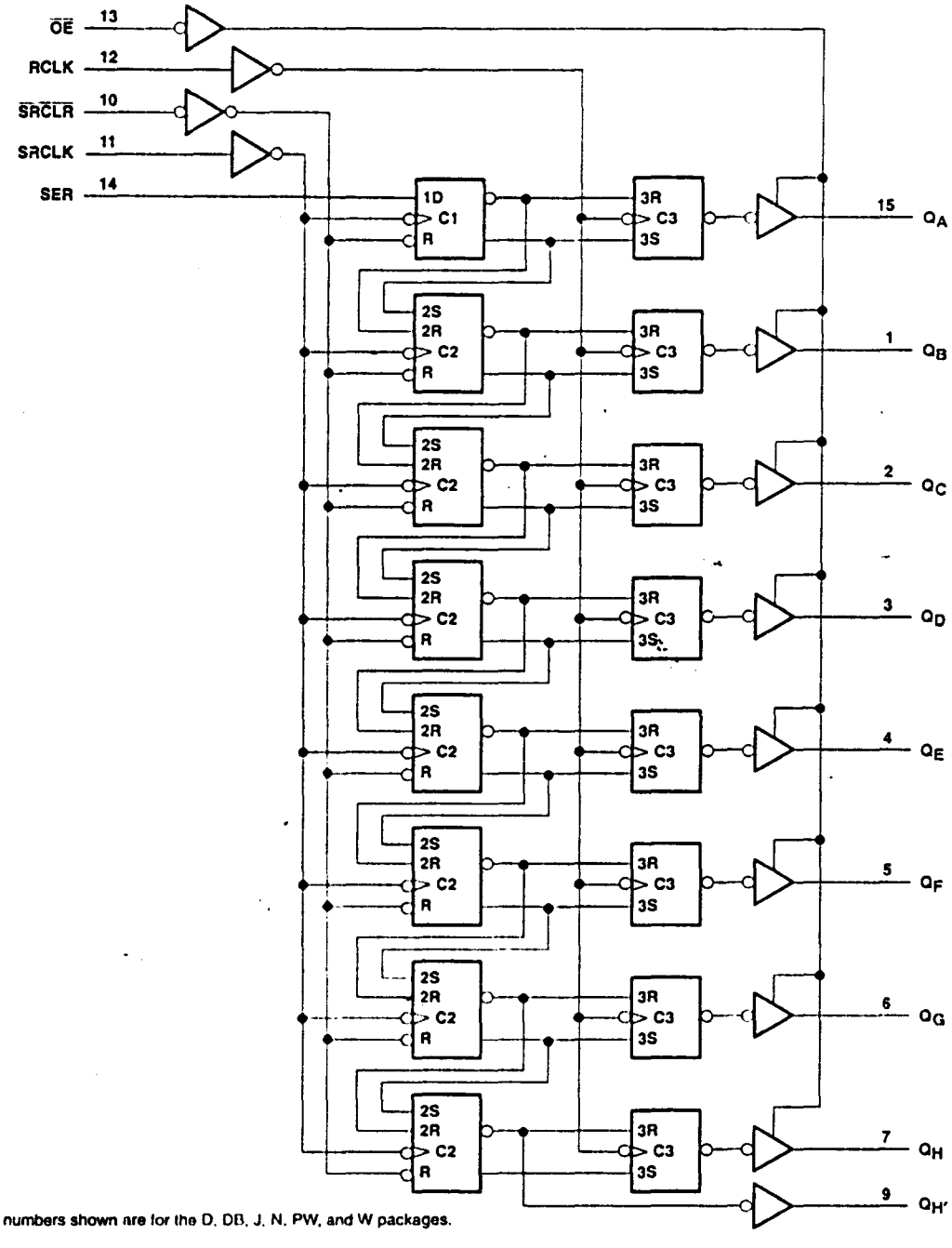
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT595		SN74AHCT595		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT595		SN74AHCT595		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHCT595		SN74AHCT595		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5		5		5		ns
		RCLK high or low	5		5		5		
		$\overline{SRCLR}$ low	5		5		5		
t_{su}	Setup time	SER before SRCLK↑	3		3		3		ns
		SRCLK↑ before RCLK↑†	5		5		5		
		$\overline{SRCLR}$ low before RCLK↑	5		5		5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.5		2.5		2.5		
t_h	Hold time	SER after SRCLK↑	2		2		2		ns
		SRCLK↑ after RCLK↑	0		0		0		
		$\overline{SRCLR}$ low after RCLK↑	0		0		0		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT595					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*	135	185		115		MHz
			C_L = 50 pF	95	155		85		
t_{PLH}*	RCLK	Q_A–Q_H	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	
t_{PLH}*	SRCLK	$Q_{H'}$	C_L = 15 pF		6.2	8.2	1	9.4	ns
t_{PHL}*					6.2	8.2	1	9.4	
t_{PHL}*	$\overline{SRCLR}$	$C_{H'}$	C_L = 15 pF		5.9	8	1	9.1	ns
t_{PZH}*	$\overline{OE}$	Q_A–Q_H	C_L = 15 pF		4.8	8.6	1	10	ns
t_{PZL}*					4.8	8.6	1	10	
t_{PHZ}*	$\overline{OE}$	Q_A–Q_H	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		6.9	9.4	1	10.5	ns
t_{PHL}					6.9	9.4	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		7.7	10.2	1	11.4	ns
t_{PHL}					7.7	10.2	1	11.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF		7.4	10	1	11.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H	C_L = 50 pF		8.3	10.6	1	12	ns
t_{PZL}					8.3	10.6	1	12	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H	C_L = 50 pF		7.6	10.3	1	11	ns
t_{PLZ}					7.6	10.3	1	11	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT595 T_A = 25°C MIN	TYP	MAX	SN74AHCT595 MIN	SN74AHCT595 MAX	UNIT
f_{max}			C_L = 15 pF	135	185		115		MHz
			C_L = 50 pF	95	155		85		
t_{PLH}	RCLK	Q_A–Q_H	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF		6.2	8.2	1	9.4	ns
t_{PHL}					6.2	8.2	1	9.4	
t_{PHL}	SRCLR	$Q_{H'}$	C_L = 15 pF		5.9	8	1	9.1	ns
t_{PZH}	OE	Q_A–Q_H	C_L = 15 pF		4.8	8.6	1	10	ns
t_{PZL}					4.8	8.6	1	10	
t_{PHZ}	OE	Q_A–Q_H	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		6.9	9.4	1	10.5	ns
t_{PHL}					6.9	9.4	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		7.7	10.2	1	11.4	ns
t_{PHL}					7.7	10.2	1	11.4	
t_{PHL}	SRCLR	$Q_{H'}$	C_L = 50 pF		7.4	10	1	11.1	ns
t_{PZH}	OE	Q_A–Q_H	C_L = 50 pF		8.3	10.6	1	12	ns
t_{PZL}					8.3	10.6	1	12	
t_{PHZ}	OE	Q_A–Q_H	C_L = 50 pF		7.6	10.3	1	11	ns
t_{PLZ}					7.6	10.3	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT595 T_A = 25°C MIN	MAX	SN74AHCT595 MIN	MAX	UNIT
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

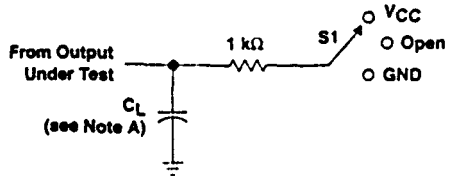
PARAMETER		SN74AHCT595 MIN	SN74AHCT595 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

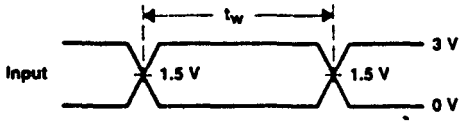
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION

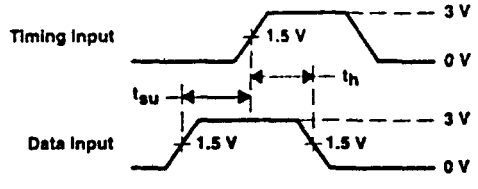


LOAD CIRCUIT

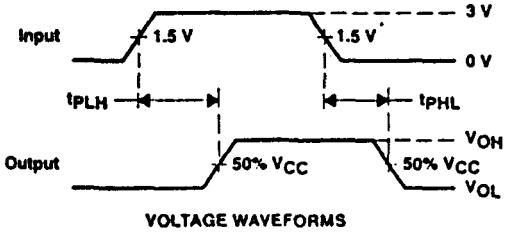
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



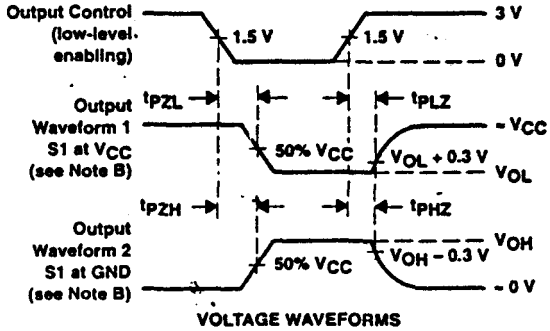
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



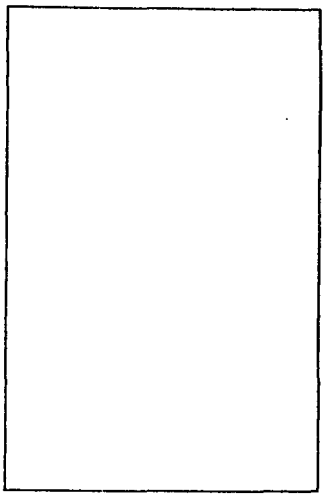
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

BIODATA



NAMA	: RONALDUS FANCY D.
NRP	: 5103096056
TEMPAT / TGL LAHIR	: RUTENG-FLORES, 21 NOVEMBER 1976
ALAMAT	: JL. RUNGKUT ASRI BARAT 1/54 SURABAYA
NO. TELEPON	: 8706629

RIWAYAT PENDIDIKAN :

- TAHUN 1990 LULUS SDK KUMBA I RUTENG
- TAHUN 1993 LULUS SMPK IMMACULATA RUTENG
- TAHUN 1996 LULUS SMA NEGERI 17 SURABAYA
- TAHUN 2001 LULUS SARJANA FAKULTAS TEKNIK JURUSAN TEKNIK ELEKTRO UNIVERSITAS KATOLIK WIDYA MANDALA