BAB V

KESIMPULAN DAN SARAN

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5.1 KESIMPULAN

Berdasarkan hasil pengamatan dan pengujian yang dilakukan terhadap ekualiseri dan sistem efek distorsi , maka dapat diambil kesimpulan diantarannya :

1. Pengujian rangkaian efek distorsi sudah tampak pada tampilan *oscilloscope* yang menunjukan adanya pemangkasan gelombang pucak dan lembah yang melebihi batas kerja dari dioda *germanium* pada inputan *tone control*.
2. Hasil pengukuran masing-masing kanal ekualiser menunjukan adanya penambahan penguatan pada *output* yang dihasilkan. Hal ini menunjukan rangkaian *analog switch* yang disusun bisa bekerja dengan masksimal. Namum, pada *level* nol masih menunjukan penguatan yang. Hal ini disebabkan besarnya tahanan (R) maksimal (memiliki penguatan terendah) tidak mampu melemahkan *sinyal input* yang ditapis.
3. Perubahan level pada tiap-tiap kanal belum menunjukan perubahan yang dapat terdengar jelas, hal ini disebabkan karena *resistor-resistor* yang dipilih oleh *analog switch* tidak menunjukan harga yang sesuai harga nyata dari jumlahan resistor-resistor tersebut.

5.2. SARAN SARAN

Alat hasil penelitian ini sebaiknya lebih cocok untuk gitar-gitar *rithem* dan melodi yang mempunyai frekuensi 16 Hz sampai 4Khz. Sedangkan Ekualiser yang dikontrol secara digital ini bisa juga diberi input lain misanya *tape*, radio,dan sebagainya asalkan mempunyai *range* frekuensi yang sama dengan ekualiser ini.

DAFTAR PUSTAKA

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3. ***Embedded controller handbook***, Vol. 1 Intel Corp., **1988**

4. Howard, M.B and Frank, C., JR., " ***Fundamentals Of Operational Amplifiers and Linear Intergrated Circuit***" ., Merril Publishing Company., 1992

5. ***MCS-51 Family User'Manual***, 1994

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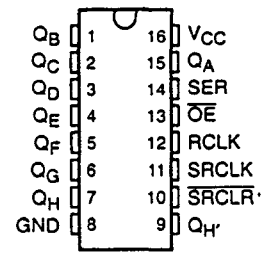
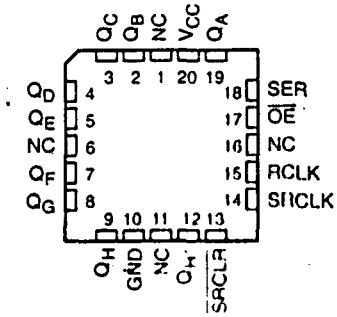
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **8-Bit Serial-In, Parallel-Out Shift**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT595 . . . J OR W PACKAGE
SN74AHCT595 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT595 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

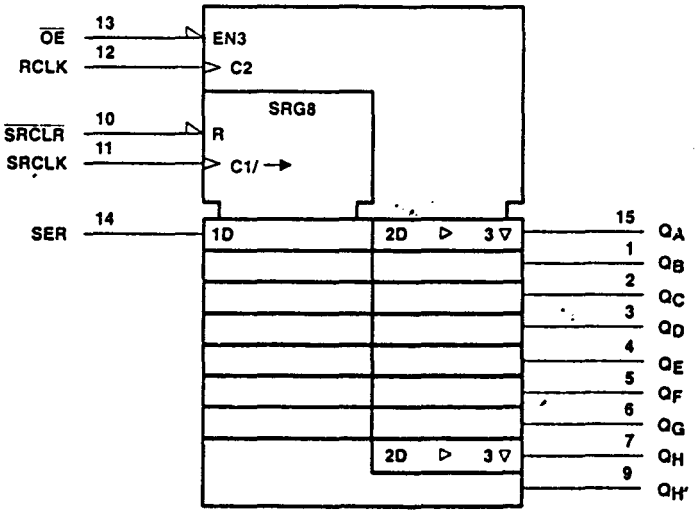
Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The SN54AHCT595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT595 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

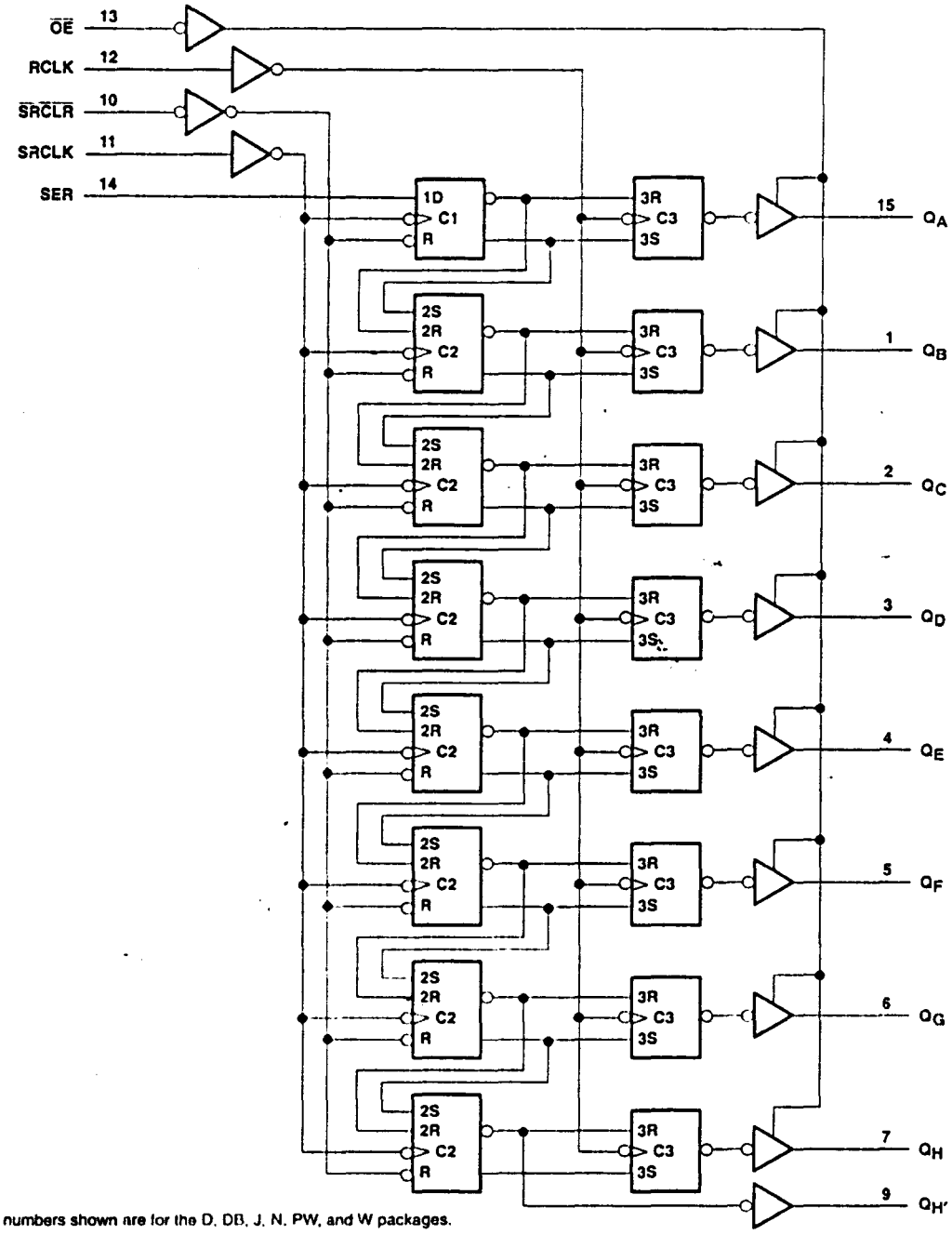
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT595		SN74AHCT595		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT595		SN74AHCT595		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHCT595		SN74AHCT595		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5		5		5		ns
		RCLK high or low	5		5		5		
		$\overline{SRCLR}$ low	5		5		5		
t_{su}	Setup time	SER before SRCLK↑	3		3		3		ns
		SRCLK↑ before RCLK↑†	5		5		5		
		$\overline{SRCLR}$ low before RCLK↑	5		5		5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.5		2.5		2.5		
t_h	Hold time	SER after SRCLK↑	2		2		2		ns
		SRCLK↑ after RCLK↑	0		0		0		
		$\overline{SRCLR}$ low after RCLK↑	0		0		0		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT595					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF*	135	185		115		MHz
			C_L = 50 pF	95	155		85		
t_{PLH}*	RCLK	Q_A–Q_H	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	
t_{PLH}*	SRCLK	$Q_{H'}$	C_L = 15 pF		6.2	8.2	1	9.4	ns
t_{PHL}*					6.2	8.2	1	9.4	
t_{PHL}*	$\overline{SRCLR}$	$C_{H'}$	C_L = 15 pF		5.9	8	1	9.1	ns
t_{PZH}*	$\overline{OE}$	Q_A–Q_H	C_L = 15 pF		4.8	8.6	1	10	ns
t_{PZL}*					4.8	8.6	1	10	
t_{PHZ}*	$\overline{OE}$	Q_A–Q_H	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		6.9	9.4	1	10.5	ns
t_{PHL}					6.9	9.4	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		7.7	10.2	1	11.4	ns
t_{PHL}					7.7	10.2	1	11.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF		7.4	10	1	11.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H	C_L = 50 pF		8.3	10.6	1	12	ns
t_{PZL}					8.3	10.6	1	12	
t_{PHZ}	$\overline{OE}$	Q_A–Q_H	C_L = 50 pF		7.6	10.3	1	11	ns
t_{PLZ}					7.6	10.3	1	11	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT595 T_A = 25°C MIN	TYP	MAX	SN74AHCT595 MIN	SN74AHCT595 MAX	UNIT
f_{max}			C_L = 15 pF	135	185		115		MHz
			C_L = 50 pF	95	155		85		
t_{PLH}	RCLK	Q_A–Q_H	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF		6.2	8.2	1	9.4	ns
t_{PHL}					6.2	8.2	1	9.4	
t_{PHL}	SRCLR	$Q_{H'}$	C_L = 15 pF		5.9	8	1	9.1	ns
t_{PZH}	OE	Q_A–Q_H	C_L = 15 pF		4.8	8.6	1	10	ns
t_{PZL}					4.8	8.6	1	10	
t_{PHZ}	OE	Q_A–Q_H	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		6.9	9.4	1	10.5	ns
t_{PHL}					6.9	9.4	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		7.7	10.2	1	11.4	ns
t_{PHL}					7.7	10.2	1	11.4	
t_{PHL}	SRCLR	$Q_{H'}$	C_L = 50 pF		7.4	10	1	11.1	ns
t_{PZH}	OE	Q_A–Q_H	C_L = 50 pF		8.3	10.6	1	12	ns
t_{PZL}					8.3	10.6	1	12	
t_{PHZ}	OE	Q_A–Q_H	C_L = 50 pF		7.6	10.3	1	11	ns
t_{PLZ}					7.6	10.3	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT595 T_A = 25°C MIN	MAX	SN74AHCT595 MIN	MAX	UNIT
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

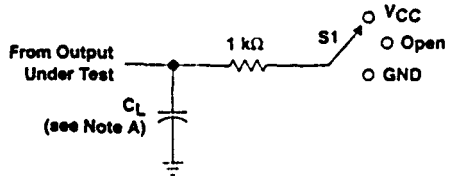
PARAMETER		SN74AHCT595 MIN	SN74AHCT595 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

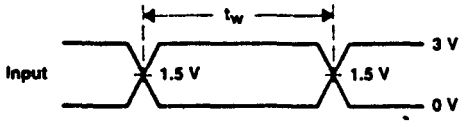
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION

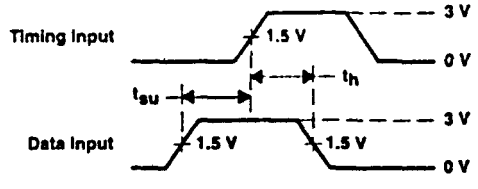


LOAD CIRCUIT

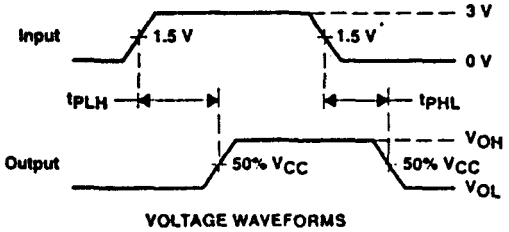
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



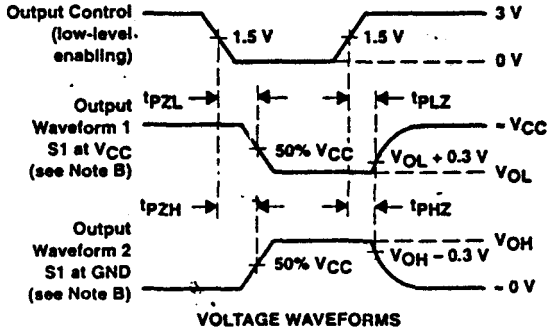
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



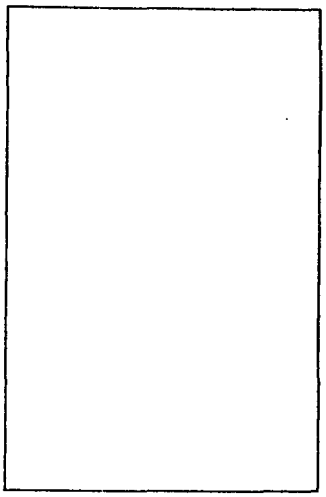
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

BIODATA



NAMA	: RONALDUS FANCY D.
NRP	: 5103096056
TEMPAT / TGL LAHIR	: RUTENG-FLORES, 21 NOVEMBER 1976
ALAMAT	: JL. RUNGKUT ASRI BARAT 1/54 SURABAYA
NO. TELEPON	: 8706629

RIWAYAT PENDIDIKAN :

- TAHUN 1990 LULUS SDK KUMBA I RUTENG
- TAHUN 1993 LULUS SMPK IMMACULATA RUTENG
- TAHUN 1996 LULUS SMA NEGERI 17 SURABAYA
- TAHUN 2001 LULUS SARJANA FAKULTAS TEKNIK JURUSAN TEKNIK ELEKTRO UNIVERSITAS KATOLIK WIDYA MANDALA