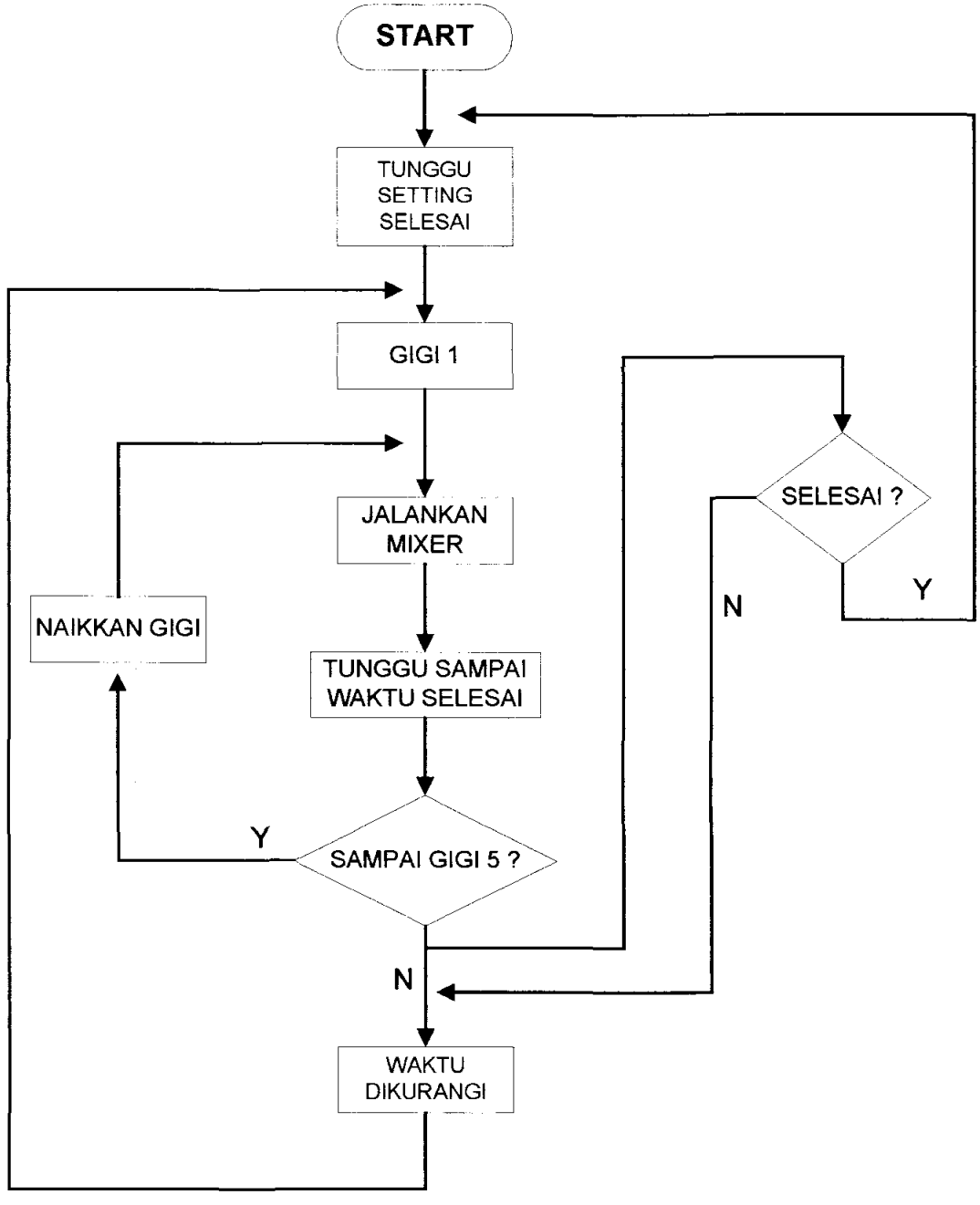
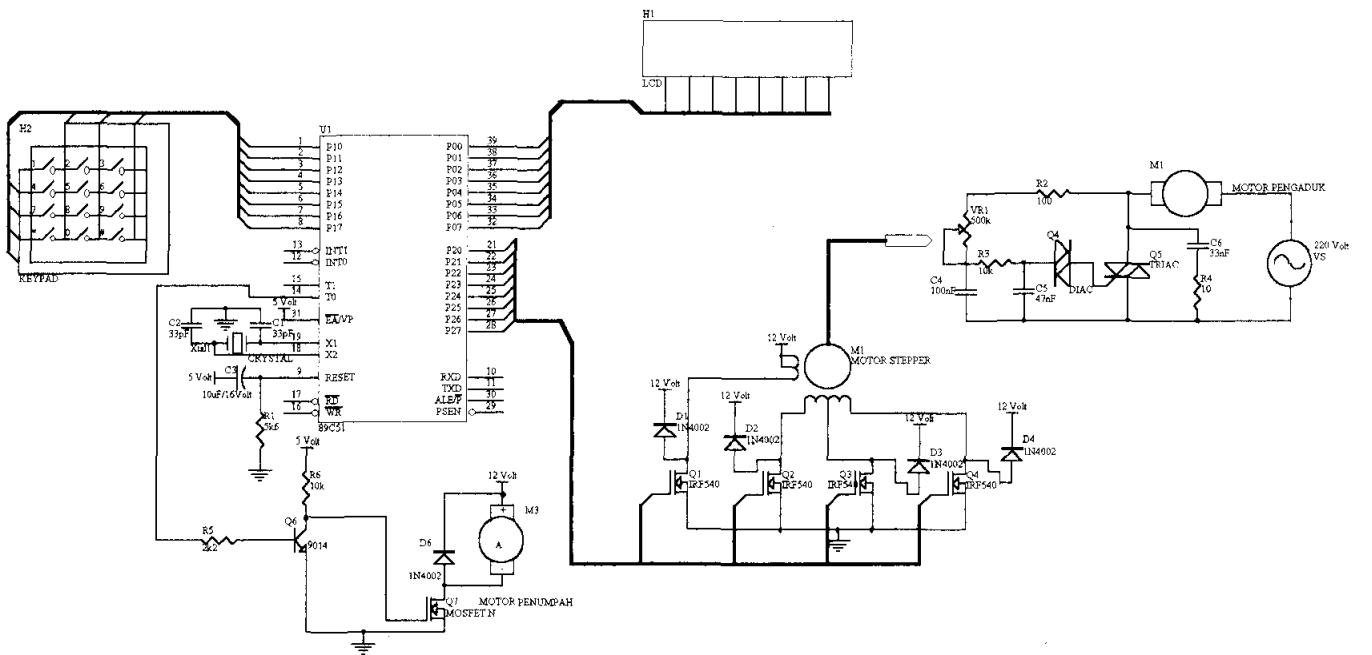
LAMPIRAN

FLOWCHART ALAT PENGADUK MENGGUNAKAN MIKROKONTROLLER





Title		
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```
;-------------------------------------------------------------------------
;P0  = LCD
;P1  = KEYPAD
;P2  = STEPPER
;P3.3 = SENSOR RPM (OPTOCOUPLER SENSOR)
;P3.4 = SOLENOID
;
;SELECT 0 = STANDBY (DO IT)
;SELECT 1 = SETING SPEED1
;SELECT 2 = SETING TIMER1
;SELECT 3 = SETING SPEED2
;SELECT 4 = SETING TIMER2
;SELECT 5 = SETING SPEED3
;SELECT 6 = SETING TIMER3
;SELECT 7 = SETING SPEED4
;SELECT 8 = SETING TIMER4
;SELECT 9 = SETING SPEED5
;SELECT 10 = SETING TIMER5
;
;-------------------------------------------------------------------------
COUNT           EQU  08H
TEMP1           EQU  09H
TEMP2           EQU  0AH
TEMP3           EQU  0BH
TEMP4           EQU  0CH
IN1         EQU  0DH
IN2         EQU  0EH
IN3         EQU  0FH
IN4         EQU  10H
VAR6        EQU  11H        ;VARIABEL 64 BIT
VAR7        EQU  12H
VAR8        EQU  13H
VAR9        EQU  14H
VAR10           EQU  15H
VAR11           EQU  16H
VAR12           EQU  17H          ;MSB 64 BIT
VAR1            EQU  18H        ;LSB 32 BIT
VAR2        EQU  19H
VAR3        EQU  1AH
VAR4        EQU  1BH        ;MSB 32 BIT
VAR5        DATA  21H       ;LSB 64 BIT
SCAN        EQU  1CH
KEY         EQU  1DH
```

```
TEMP_KEYPAD     EQU  1EH   ;GENERAL REGISTER
FREE        EQU  1FH
RAMDIS          EQU  30H   ;RAM DISPLAY 5 BYTES
SELECT          EQU  35H
SPEED1          EQU  36H
SPEED2          EQU  38H
SPEED3          EQU  3AH
SPEED4          EQU  3CH
SPEED5          EQU  3EH
TIMER1          EQU  40H
TIMER2          EQU  41H
TIMER3          EQU  42H
TIMER4          EQU  43H
TIMER5          EQU  44H
MENIT           EQU  45H
SECON1          EQU  46H
SECON2          EQU  47H
SECON3          EQU  48H
POINTER         EQU  49H
ACTUAL_SPEED1   EQU  4AH
ACTUAL_SPEED2   EQU  4BH
PRESENT_SPEED1  EQU  4CH
PRESENT_SPEED2  EQU  4DH
NOW_SPEEDEQU    24H   ;2 BYTES
RPM1        EQU  4EH
RPM2        EQU  4FH
RPM3        EQU  22H
STEPER          EQU  23H
DELAY1          EQU  24H
DELAY2          EQU  25H
ULANG           EQU  26H
KEYPRESS    BIT  0
DO_IT       BIT  1
RPM_OK          BIT  2
HIT_RPM_OK      BIT  3
STEP_UPPERBIT  4

            ORG  00H
            AJMP START

            ORG  1BH
            AJMP MINUTE
```

```
            ORG  30H
;--------------------------------
;     INTERUPT MENIT
;--------------------------------
MINUTE          PUSH PSW
            PUSH A
            PUSH 0
            PUSH B
            DJNZ SECON1,ESC_MINUTE
            MOV  A,ULANG
            CJNE A,#1,PASS_200
            MOV  SECON1,#100
            SJMP PASS_MNT

PASS_200    MOV  SECON1,#200
PASS_MNT    DJNZ SECON2,ESC_MINUTE
            MOV  SECON2,#24
            DJNZ SECON3,ESC_MINUTE
            MOV  SECON3,#60
            DJNZ MENIT,ESC_MINUTE
            INC  POINTER
            MOV  A,#TIMER1
            ADD  A,POINTER
            MOV  R0,A
            MOV  MENIT,@R0

            MOV  A,POINTER
            CJNE A,#5,EXECUTE
            CLR  TR1
            CLR  DO_IT
            CLR  P3.4           ;TUANGKAN TEPUNG
            INC  ULANG
            MOV  B,#200
OFF_MOTORACALL      STEPER_KIRI
            ACALL       DELAY_STEP
            DJNZ B,OFF_MOTOR
            MOV  B,#100
WAIT_DELAY      ACALL       DELAY_STEP      ;DELAY WAIT
            DJNZ B,WAIT_DELAY
            MOV  ACTUAL_SPEED1,#0
            MOV  ACTUAL_SPEED2,#0
            SJMP ESC_MINUTE
```

```
EXECUTE         MOV  A,POINTER
                RL   A
                ADD  A,#SPEED1
                MOV  R0,A
                MOV  A,@R0
                SUBB A,ACTUAL_SPEED1
                MOV  B,A
SHIFT_RIGHT     ACALL      STEPER_KANAN
                ACALL      DELAY_STEP
                DJNZ B,SHIFT_RIGHT
                MOV  ACTUAL_SPEED1,@R0

ESC_MINUTE      POP  B
                POP  0
                POP  A
                POP  PSW
                RETI

;----------------------
;   DELAY STEPER
;----------------------
DELAY_STEP      MOV  DELAY1,#30
DEL_STEP   MOV  DELAY2,#250
                DJNZ DELAY2,$
                DJNZ DELAY1,DEL_STEP
                RET

;--------------------------------
;               DEFAULT
;--------------------------------
DEFAULT         MOV  P2,#0          ;ALL STEPER DRIVER OFF
                MOV  R7,#32
                MOV  R0,#RAMDIS
RESET           MOV  @R0,#0
                INC  R0
                DJNZ R7,RESET
                MOV  SELECT,#1
                MOV  TMOD,#22H
                MOV  TL1,#64
                MOV  TH1,#64
                MOV  TL0,#72
                MOV  TH0,#72
                SETB IT1
```

```
                MOV  IE,#88H
                CLR  TR1
                MOV  STEPER,#33H
                RET

;--------------------------------
;       DELAY 4 mS
;--------------------------------
DELAY4M     MOV   R7,#10
DEL4M       MOV   R6,#250
            DJNZ  R6,$
            DJNZ  R7,DEL4M
            RET

;-----------------------------
;      ENABLE PULSE
;-----------------------------
ENABLE       ANL   A,#0FH
             MOV   P0,A
             ORL   A,#20H
             MOV   P0,A
             ANL   A,#0FH
             MOV   P0,A
             ACALL DELAY4M
             RET

;-----------------------------
;      CONTROL LCD
;-----------------------------
LCDCONTROL    MOV   FREE,A
              SWAP  A
              ACALL ENABLE
              MOV   A,FREE
              ACALL ENABLE
              RET

;-----------------------------
;   INISILISASI LCD 4 BIT
;---
NEXTDIGIT
              AJMP ESC_DISPLAY

DISP_TIMER MOV  A,#0CAH              ;LINE 1 KOLOM 7
```

```
                ACALL       LCDCONTROL
                MOV  R5,#2
                MOV  R0,#RAMDIS+1
NEXTDIGIT_TMR   MOV  A,@R0
                ORL  A,#30H
                ACALL       LCD
                DEC  R0
                DJNZ R5,NEXTDIGIT_TMR
ESC_DISPLAY     RET

;-------------------------
;  LOAD_NULL OF RAMDIS
;-------------------------
LOAD_NULLMOV  RAMDIS+2,#0
                MOV  RAMDIS+3,#0
                MOV  RAMDIS+4,#0
                RET

;-------------------------
;LOADING CONTENT OF RAMDIS
;-------------------------
LOADING_DISP    MOV  DPTR,#LOAD_RAMDIS

SELECT1
                AJMP SELECT2
                AJMP SELECT3
                AJMP SELECT4
                AJMP SELECT5
                AJMP SELECT6
                AJMP SELECT7
                AJMP SELECT8
                AJMP SELECT9
                AJMP SELECT10

;---------------------
;   MOTOR _OFF
;---------------------
MOTOR_OFFMOV  R6,#120
MOTOR_OFF_NEXT      ACALL       STEPER_KIRI
                ACALL       DELAY_STEP
                DJNZ R6,MOTOR_OFF_NEXT
                RET
```

```
;---------------------SELECT0
SELECT0         JB      DO_IT,PASS_SELECT0
                MOV  A,ULANG
                CJNE  A,#2,MOTOR_ON             ;CEK END SYSTEM
                ACALL       MOTOR_OFF
                MOV  A,#80H
                ACALL       LCDCONTROL
                MOV  DPTR,#STAND_BY
                MOV  R6,#16
DISP1           CLR  A
                MOVC        A,@A+DPTR
                ACALL       LCD
                INC  DPTR
                DJNZ  R6,DISP1

                MOV  A,#0C0H
                ACALL       LCDCONTROL
                MOV  R6,#16
DISP2           CLR  A
                MOVC        A,@A+DPTR
                ACALL       LCD
                INC  DPTR
                DJNZ  R6,DISP2
WAIT_KEY        ACALL       KEYPAD
                MOV  A,SELECT
                CJNE  A,#1,WAIT_KEY
                AJMP PASS_SELECT0

MOTOR_ON MOV  POINTER,#0
                MOV  MENIT,TIMER1
                MOV  ACTUAL_SPEED1,SPEED1
                MOV  B,ACTUAL_SPEED1
SHIFT_START     ACALL       STEPER_KANAN
                ACALL       DELAY_STEP
                DJNZ  B,SHIFT_START
                MOV  A,ULANG
                CJNE  A,#1,SECON1_200
                MOV  SECON1,#100
                SJMP SECON_PASS
SECON1_200 MOV  SECON1,#200
SECON_PASS      MOV  SECON2,#24
                MOV  SECON3,#60
                SETB DO_IT
```

```
            SETB  TR1
PASS_SELECT0    ACALL       DISPLAY
            AJMP  BACK

;----------------------SELECT1
SELECT1             MOV  ULANG,#0
            MOV  POINTER,#0
            SETB  P3.4
            MOV  A,#80H
            ACALL       LCDCONTROL
            MOV  R6,#16
BLANK               MOV  A,#20H
            ACALL       LCD
            DJNZ  R6,BLANK
            CLR   DO_IT
            MOV  NOW_SPEED,#0
            MOV  NOW_SPEED+1,#0
            CLR   TR1
            CLR   TR0
            SETB  P3.4
            MOV  A,RAMDIS+2
            MOV  B,#100
            MUL  AB
            MOV  SPEED1+1,B
            MOV  SPEED1,A
            MOV  A,RAMDIS+1
            MOV  B,#10
            MUL  AB
            ADD  A,SPEED1
            MOV  SPEED1,A
            MOV  A,#0
            ADDC A,SPEED1+1
            MOV  SPEED1+1,A
            MOV  A,RAMDIS
            ADD  A,SPEED1
            MOV  SPEED1,A
            MOV  A,#0
            ADDC A,SPEED1+1
            MOV  SPEED1+1,A
            ACALL       DISPLAY
            AJMP  BACK

;----------------------SELECT2
```

```
SELECT2         MOV  ULANG,#0
                MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,RAMDIS
                MOV  TIMER1,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT3
SELECT3         MOV  A,RAMDIS+2
                MOV  B,#100
                MUL  AB
                MOV  SPEED2+1,B
                MOV  SPEED2,A
                MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,SPEED2
                MOV  SPEED2,A
                MOV  A,#0
                ADDC A,SPEED2+1
                MOV  SPEED2+1,A
                MOV  A,RAMDIS
                ADD  A,SPEED2
                MOV  SPEED2,A
                MOV  A,#0
                ADDC A,SPEED2+1
                MOV  SPEED2+1,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT4
SELECT4         MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,RAMDIS
                MOV  TIMER2,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT5
SELECT5         MOV  A,RAMDIS+2
```

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```
                MOV  B,#100
                MUL  AB
                MOV  SPEED3+1,B
                MOV  SPEED3,A
                MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,SPEED3
                MOV  SPEED3,A
                MOV  A,#0
                ADDC A,SPEED3+1
                MOV  SPEED3+1,A
                MOV  A,RAMDIS
                ADD  A,SPEED3
                MOV  SPEED3,A
                MOV  A,#0
                ADDC A,SPEED3+1
                MOV  SPEED3+1,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT6
SELECT6             MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,RAMDIS
                MOV  TIMER3,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT7
SELECT7             MOV  A,RAMDIS+2
                MOV  B,#100
                MUL  AB
                MOV  SPEED4+1,B
                MOV  SPEED4,A
                MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,SPEED4
                MOV  SPEED4,A
                MOV  A,#0
                ADDC A,SPEED4+1
```

```
                MOV  SPEED4+1,A
                MOV  A,RAMDIS
                ADD  A,SPEED4
                MOV  SPEED4,A
                MOV  A,#0
                ADDC A,SPEED4+1
                MOV  SPEED4+1,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT8
SELECT8              MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,RAMDIS
                MOV  TIMER4,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT9
SELECT9              MOV  A,RAMDIS+2
                MOV  B,#100
                MUL  AB
                MOV  SPEED5+1,B
                MOV  SPEED5,A
                MOV  A,RAMDIS+1
                MOV  B,#10
                MUL  AB
                ADD  A,SPEED5
                MOV  SPEED5,A
                MOV  A,#0
                ADDC A,SPEED5+1
                MOV  SPEED5+1,A
                MOV  A,RAMDIS
                ADD  A,SPEED5
                MOV  SPEED5,A
                MOV  A,#0
                ADDC A,SPEED5+1
                MOV  SPEED5+1,A
                ACALL       DISPLAY
                AJMP BACK

;----------------------SELECT10
```

```
SELECT10    MOV  A,RAMDIS+1
            MOV  B,#10
            MUL  AB
            ADD  A,RAMDIS
            MOV  TIMER5,A
            ACALL       DISPLAY
            AJMP BACK

;----------------------
;   STEPER KANAN
;----------------------
STEPER_KANAN    MOV  A,STEPER
            RL   A
            MOV  STEPER,A
            MOV  P2,STEPER
            RET

;------------------------
;       STEPER KIRI
;------------------------
STEPER_KIRI     MOV  A,STEPER
            RR   A
            MOV  STEPER,A
            MOV  P2,STEPER
            RET

;----------------------
;    MAIN PROGRAM
;----------------------
START           MOV  SP,#60H
            ACALL       DEFAULT
            MOV  B,#120
INIT_OFF    ACALL       STEPER_KIRI
            ACALL       DELAY_STEP
            DJNZ B,INIT_OFF
            ACALL       INITLCD4BIT
            ACALL       NAMA_NRP

LAGI        ACALL       KEYPAD
            ACALL       UPDATE
            AJMP LAGI

BACKGROUND      DB   '  STAND BY  '
```

```
            DB    'SPEED 1:    RPM'
            DB    'TIMER 1:    Mnt'
            DB    'SPEED 2:    RPM'
            DB    'TIMER 2:    Mnt'
            DB    'SPEED 3:    RPM'
            DB    'TIMER 3:    Mnt'
            DB    'SPEED 4:    RPM'
            DB    'TIMER 4:    Mnt'
            DB    'SPEED 5:    RPM'
            DB    'TIMER 5:    Mnt'
STAND_BY    DB    '  END SYSTEM  '
            DB    ' PRESS # KEY !! '
```

Features

- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

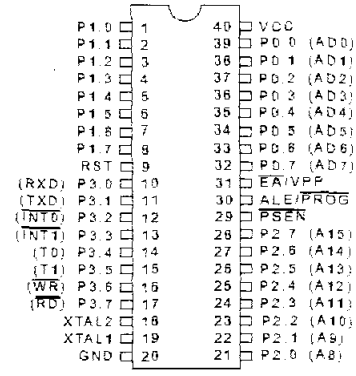
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

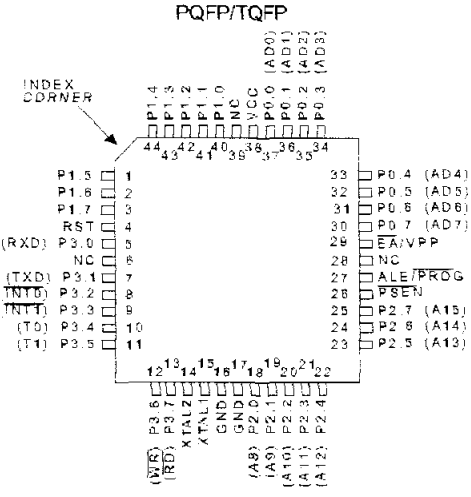
(continued)

Pin Configurations

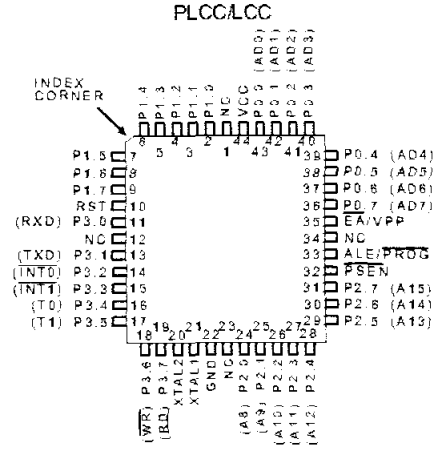
PDIP/Cerdip



PQFP/TQFP



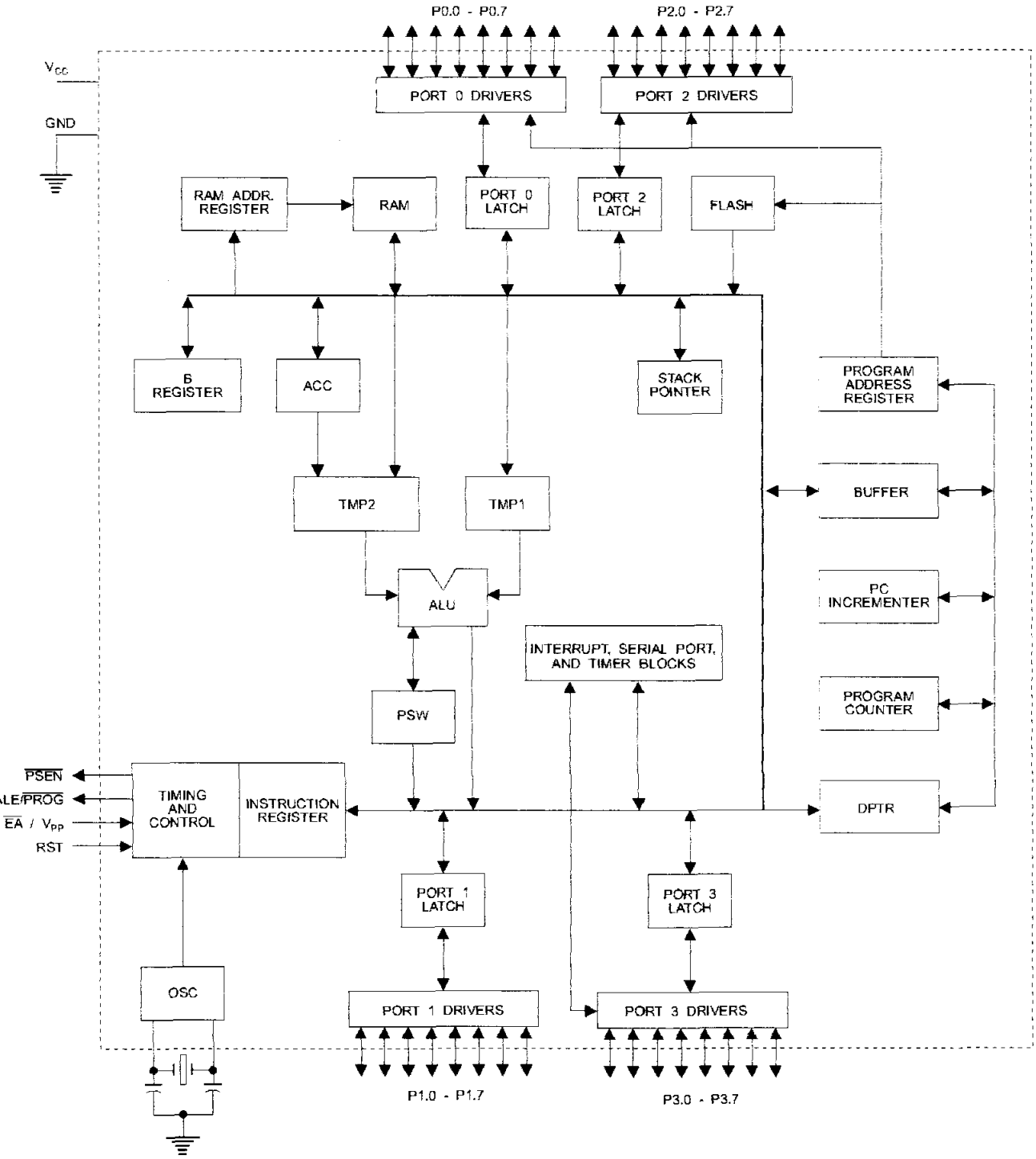
PLCC/LCC



8-Bit Microcontroller with 4 Kbytes Flash

AT89C51

Block Diagram



Description (Continued)

The AT89C51 provides the following standard features: 4 Kbytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (extenal interrupt 0)
P3.3	$\overline{INT1}$ (extenal interrupt 1)
P3.4	T0 (timer 0 extenal input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (extenal data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcrontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

(continued)

Pin Description (Continued)

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

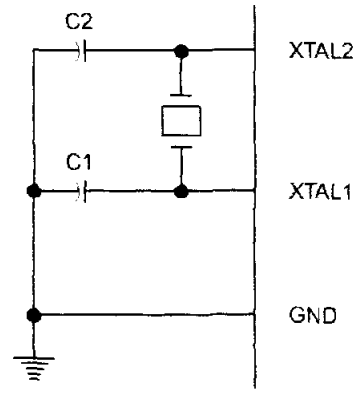
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

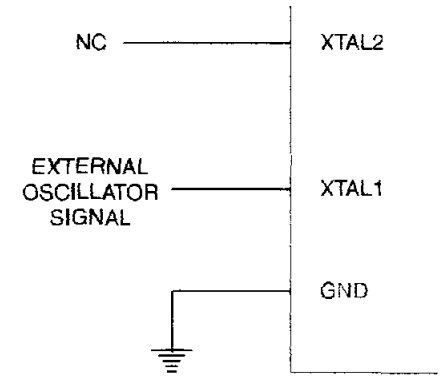
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

ware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12 V	V_{PP} = 5 V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12 V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an at-

(continued)

Programming the Flash (Continued)

empted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, nd the next cycle may begin. Data Polling may begin any me after a write cycle has been initiated.

eady/Busy: The progress of byte programming can lso be monitored by the RDY/BSY output signal. P3.4 is ulled low after ALE goes high during programming to inicate BUSY. P3.4 is pulled high again when programing is done to indicate READY.

rogram Verify: If lock bits LB1 and LB2 have not been rogrammed, the programmed code data can be read ack via the address and data lines for verification. The ock bits cannot be verified directly. Verification of the lock its is achieved by observing that their features are enbled.

hip Erase: The entire Flash array is erased electrically y using the proper combination of control signals and by olding ALE/PROG low for 10 ms. The code array is writen with all "1"s. The chip erase operation must be exeuted before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12 V programming
(032H) = 05H indicates 5 V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L	⎍	H/12V[1]	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L	⎍	H/12V	H	H	H	H
	Bit - 2	H	L	⎍ [2]	H/12V	H	H	L	L
	Bit - 3	H	L	⎍	H/12V	H	L	H	L
Chip Erase		H	L	⎍	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

lotes: 1. The signature byte at location 032H designates whether V_{PP} = 12 V or V_{PP} = 5 V should be used to enable programming.

2. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.

igure 3. Programming the Flash

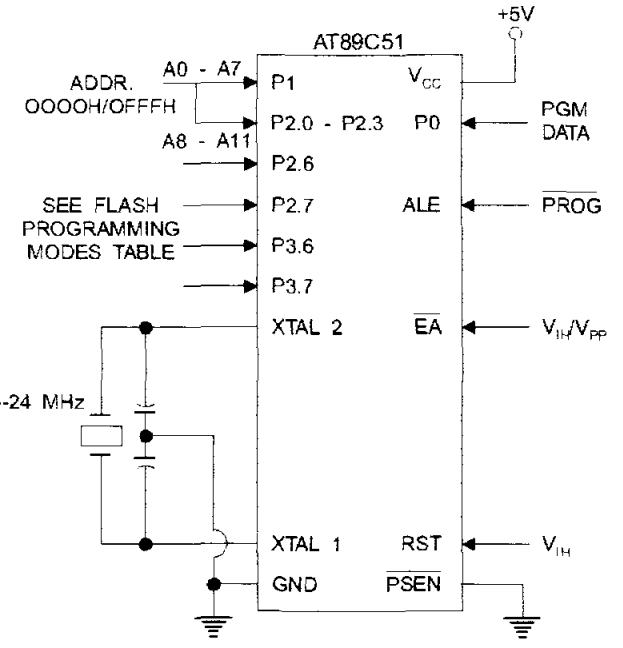
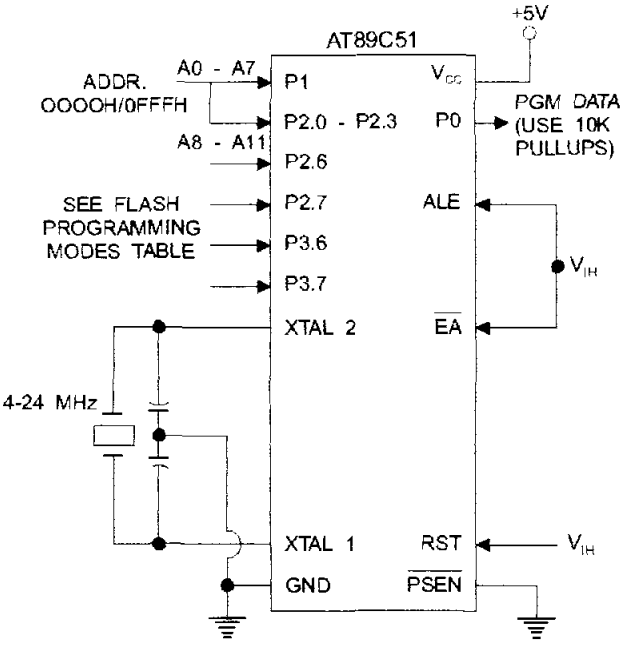


Figure 4. Verifying the Flash



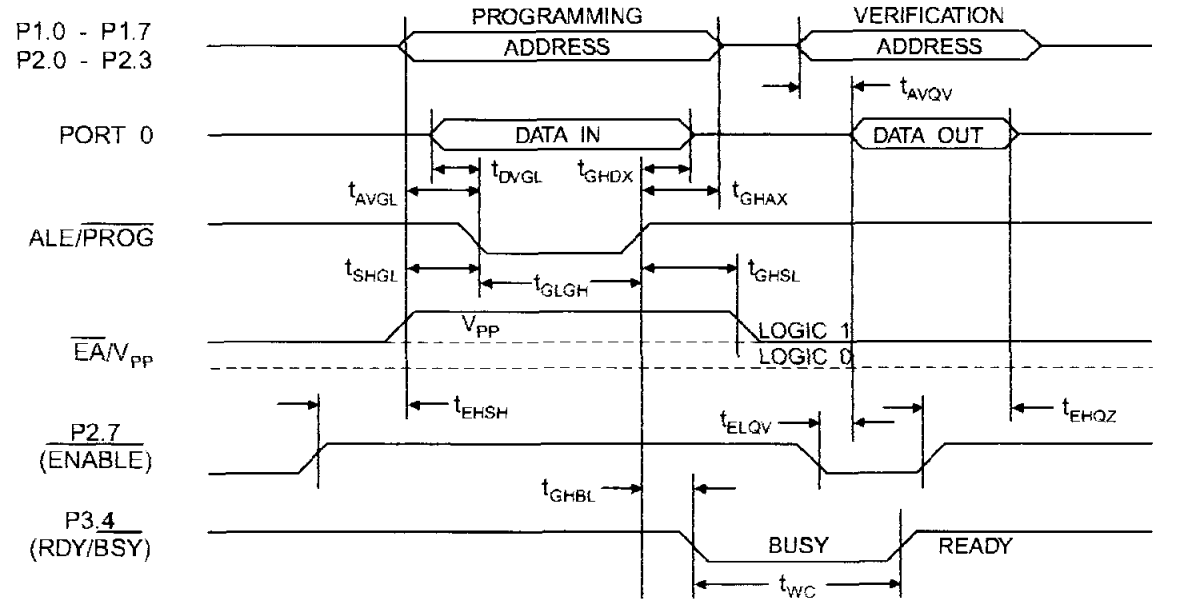
Flash Programming and Verification Characteristics

T_A = 21°C to 27°C, V_{CC} = 5.0 ± 10%

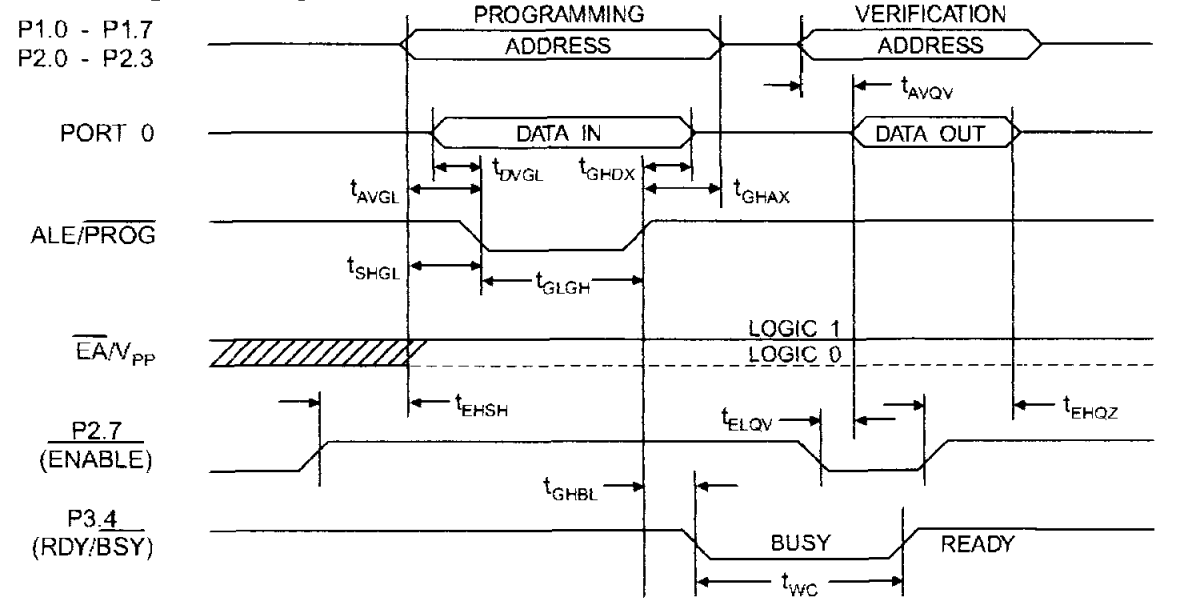
Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48tCLCL		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		48tCLCL	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQV}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

ote: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode



Flash Programming and Verification Waveforms - Low Voltage Mode



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0 V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45 V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2 V		-650	µA
I_{LI}	Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode[2]	V_{CC} = 6 V		100	µA
		V_{CC} = 3 V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin:10 mA
Maximum I_{OL} per 8-bit port:
Port 0:26 mA
Ports 1,2, 3:15 mA
Maximum total IOL for all output pins:71 mA
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum VCC for Power Down is 2 V.

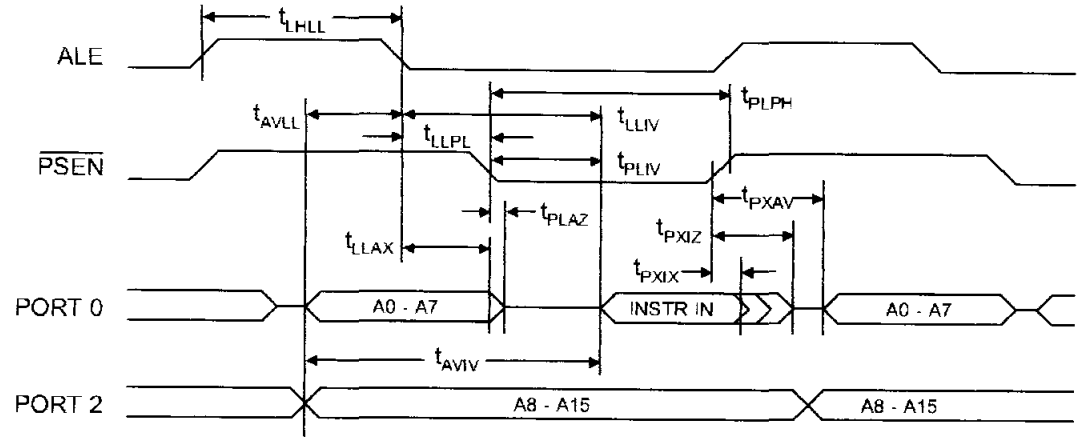
A.C. Characteristics

Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

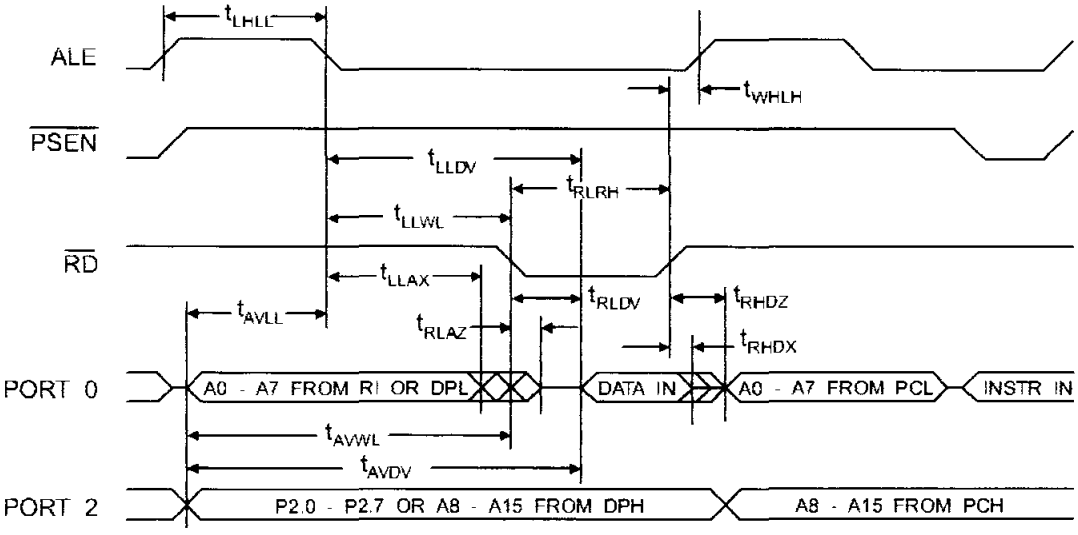
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	28		tCLCL-13		ns
t_{LLAX}	Address Hold After ALE Low	48		tCLCL-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		4tCLCL-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		8tCLCL-150	ns
t_{AVDV}	Address to Valid Data In		585		9tCLCL-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

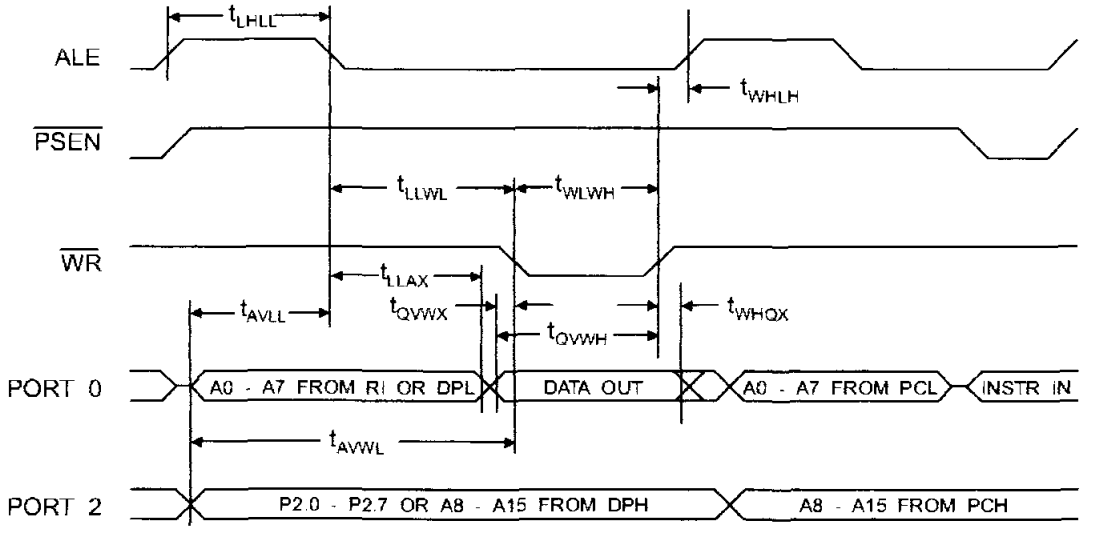
External Program Memory Read Cycle



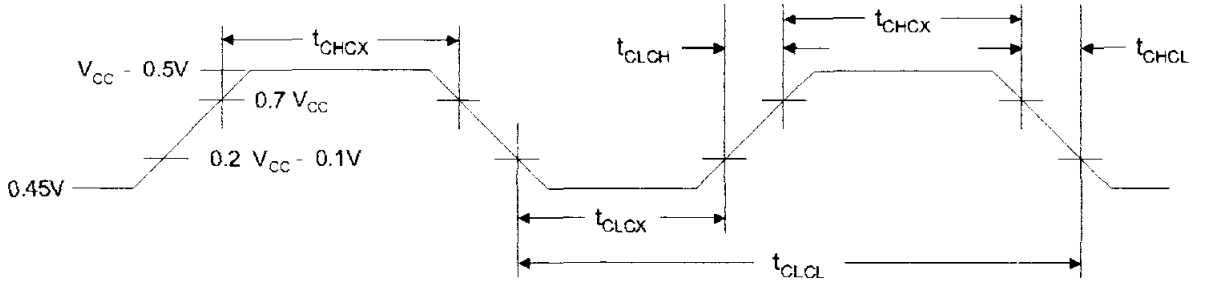
External Data Memory Read Cycle



External Data Memory Cycle



External Clock Drive Waveforms



External Clock Drive

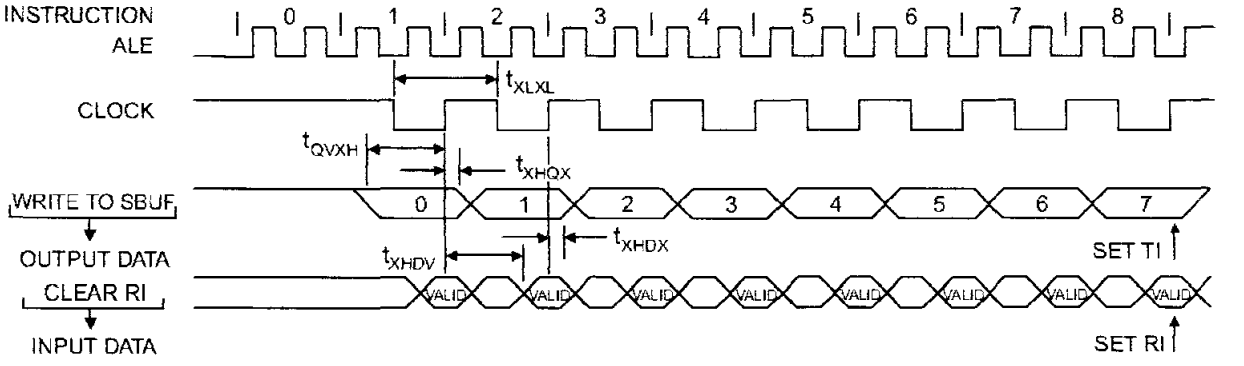
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

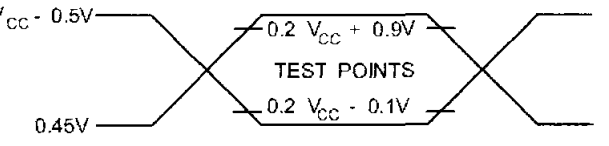
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-33		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10tCLCL-133	ns

Shift Register Mode Timing Waveforms

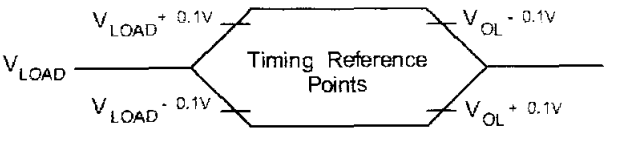


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

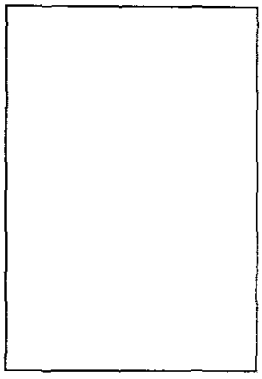
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5 V ± 20%	AT89C51-12AC AT89C51-12JC AT89C51-12PC AT89C51-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-12AI AT89C51-12JI AT89C51-12PI AT89C51-12QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C51-12AA AT89C51-12JA AT89C51-12PA AT89C51-12QA	44A 44J 40P6 44Q	Automotive (-40°C to 125°C)
	5 V ± 10%	AT89C51-12DM AT89C51-12LM	40D6 44L	Military (-55°C to 125°C)
		AT89C51-12DM/883 AT89C51-12LM/883	40D6 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
16	5 V ± 20%	AT89C51-16AC AT89C51-16JC AT89C51-16PC AT89C51-16QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-16AI AT89C51-16JI AT89C51-16PI AT89C51-16QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C51-16AA AT89C51-16JA AT89C51-16PA AT89C51-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 125°C)
20	5 V ± 20%	AT89C51-20AC AT89C51-20JC AT89C51-20PC AT89C51-20QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-20AI AT89C51-20JI AT89C51-20PI AT89C51-20QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5 V ± 20%	AT89C51-24AC AT89C51-24JC AT89C51-24PC AT89C51-24QC	44A 44J 44P6 44Q	Commercial (0°C to 70°C)
		AT89C51-24AI AT89C51-24JI AT89C51-24PI AT89C51-24QI	44A 44J 44P6 44Q	Industrial (-40°C to 85°C)

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
40D6	40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

BIODATA



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